Consorzio Nazionale Interuniversitario per la Nanoelettronica
IUNET

EMMA – Emerging Materials for Mass-storage Architectures

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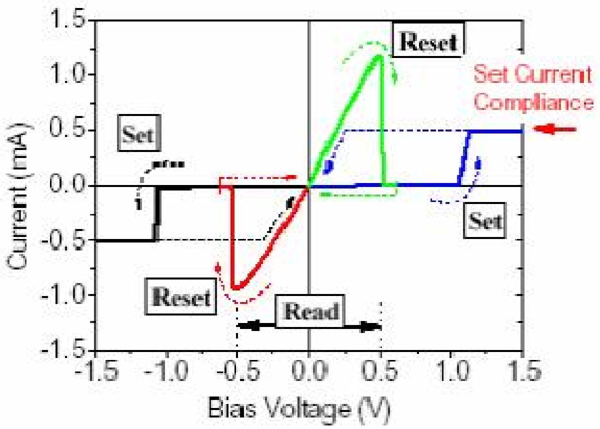
Bertinoro (FC), 24/11/2007

Resistive-switching materials and memories

- Topic = Resistive switching random access memories (RRAM)
- First observation in the 1960s [J.G. Simmons and R.R. Verderber, The Radio and Electronic Engineer, 81 (1967)]
- Recently many reports about RRAM:
  - W. W. Zhuang *et al.*, IEDM02 (Sony)
  - I. Baek *et al.*, IEDM04 (Samsung)
  - IEDM05–07: about 15 contributions on RRAM



- Resistive memories offer the potential for $4F^2$ cross-point memory cell
  à highly attractive for mass-storage application

Aim of the project

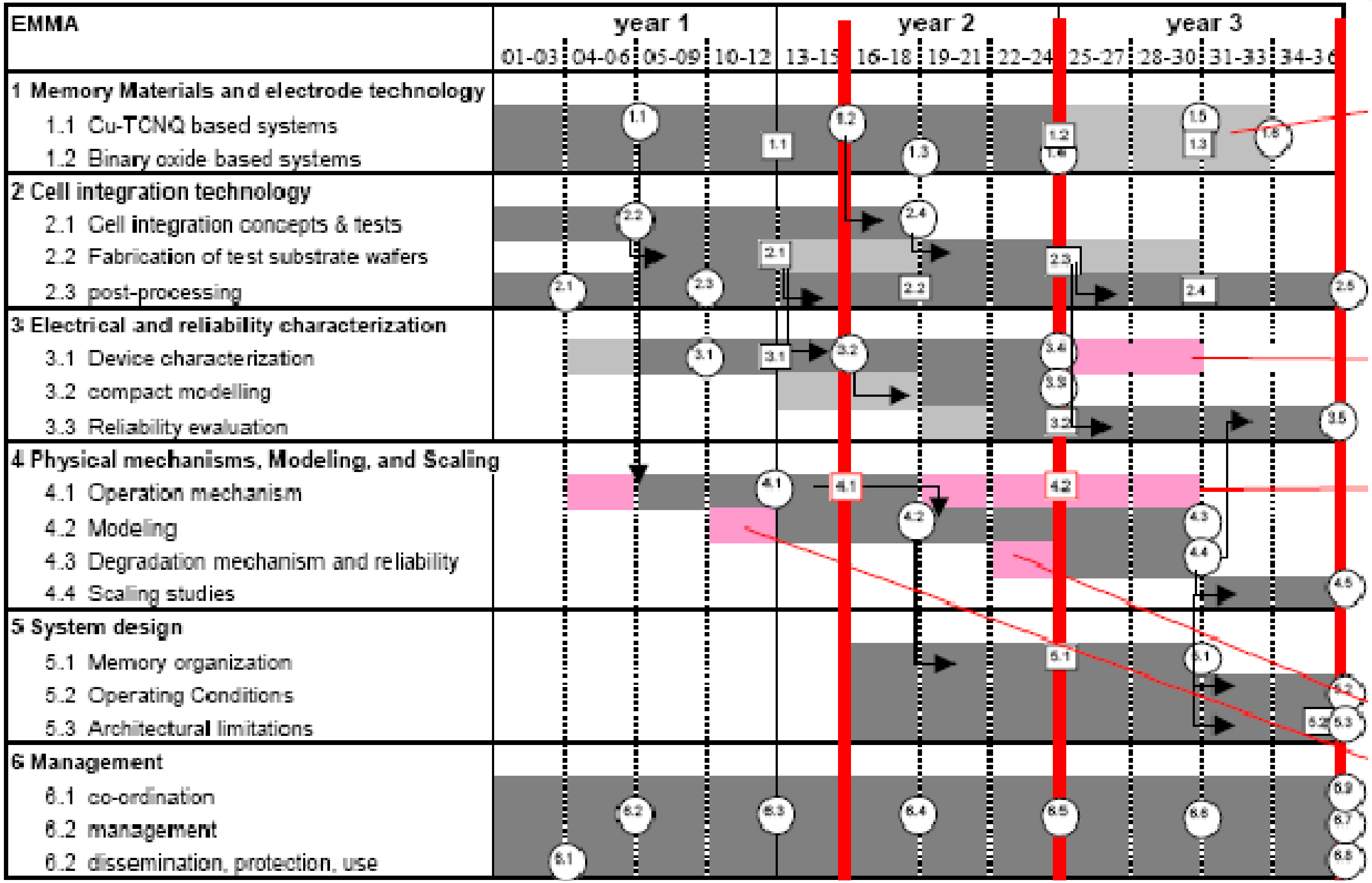
Investigate emerging non volatile memories based on resistive switching in dielectric layers:

- Materials issue (deposition, integration, process compatibility)
- Integration of RRAM cells and arrays
- Feasibility of low-voltage/low current set/reset switching
- Cell reliability (endurance, data retention)
- Physical mechanisms/models for switching and reliability
- Scaling potential (reset current, forming/set voltage)
- Feasibility of $4F^2$ cross-point architectures

The consortium

- Coordinator:
- Participants:
- Members involved:

Schedule of the project



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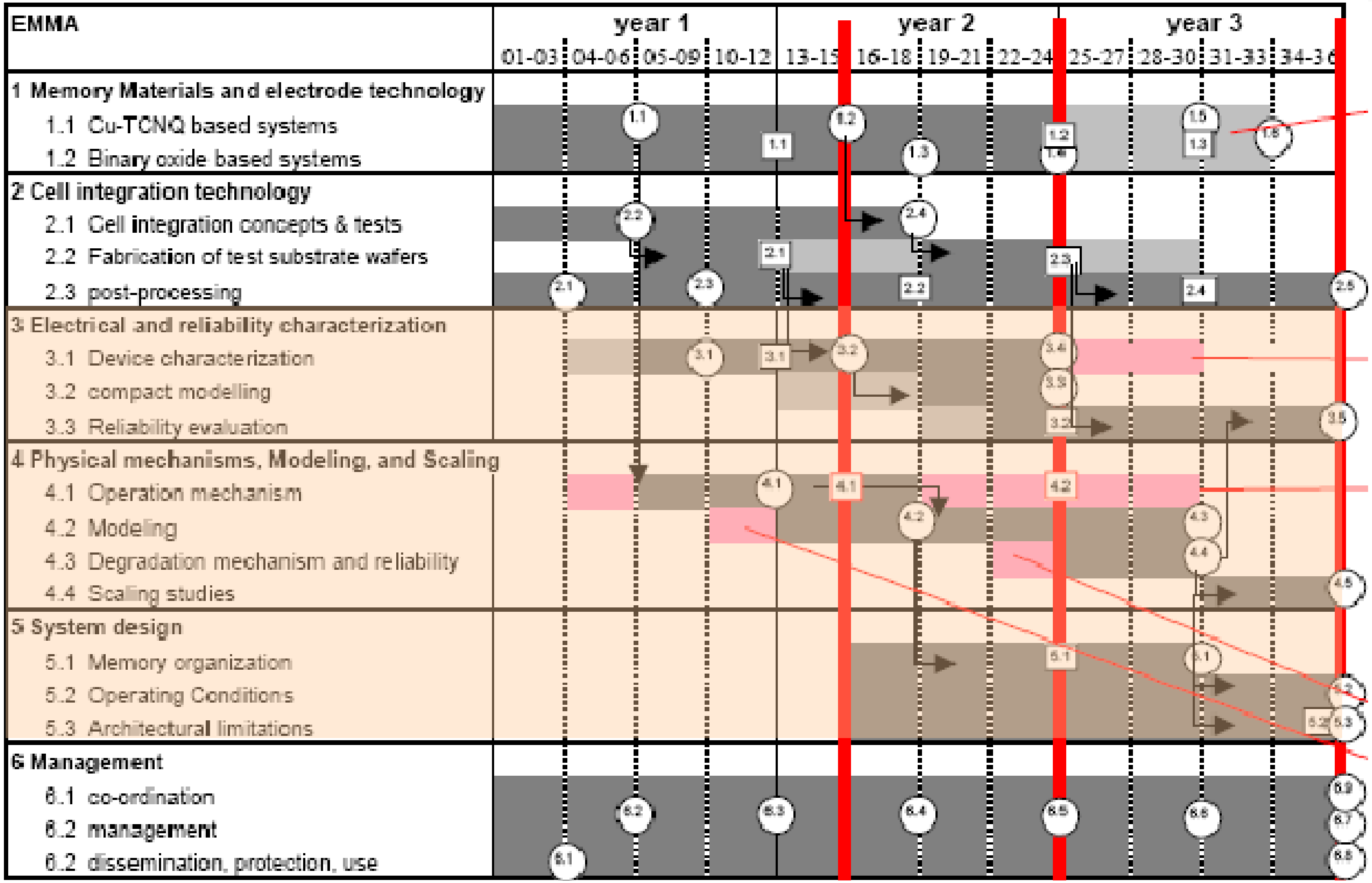
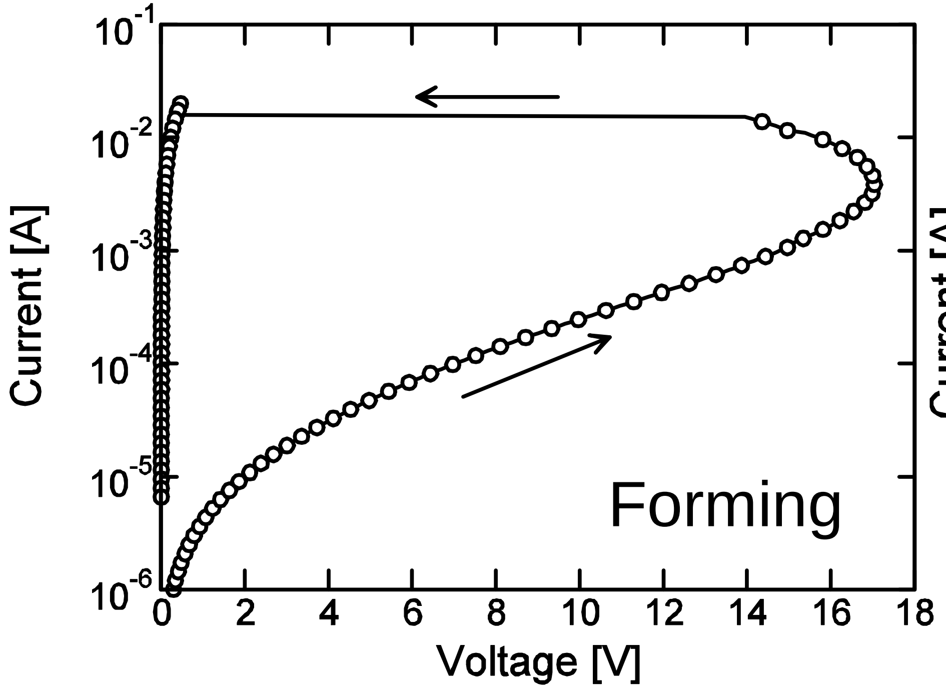
Schedule of the project

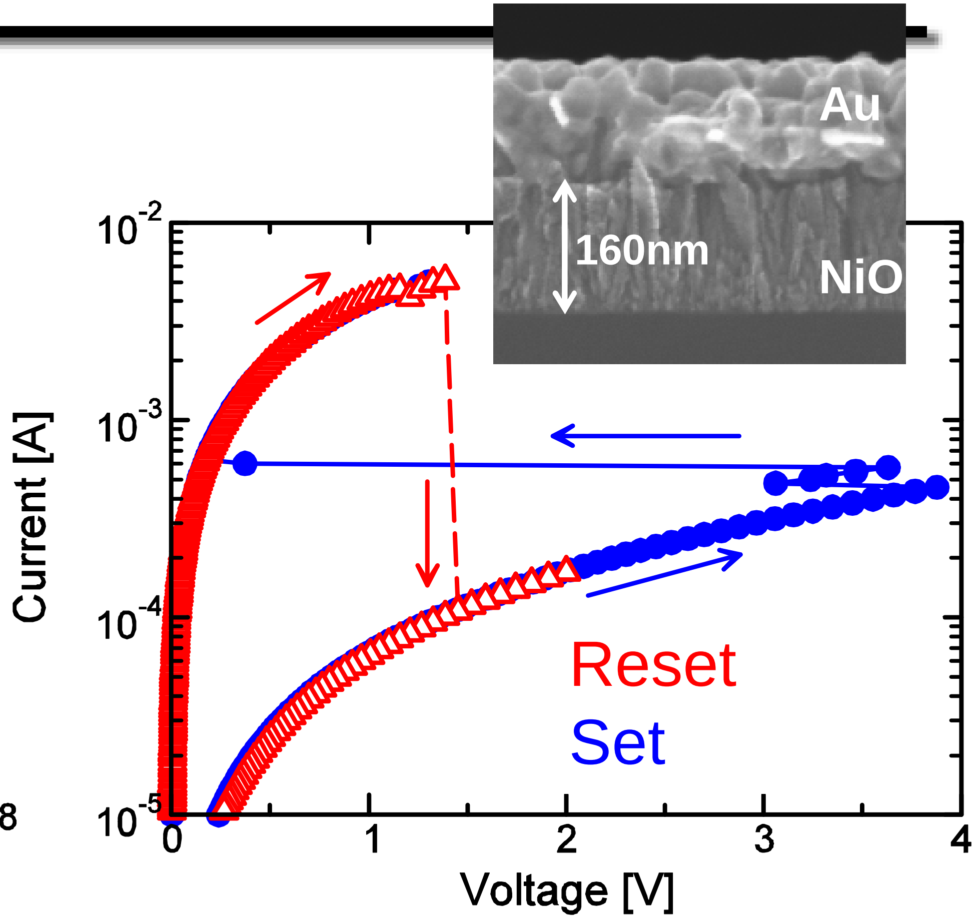


IUNET involvement

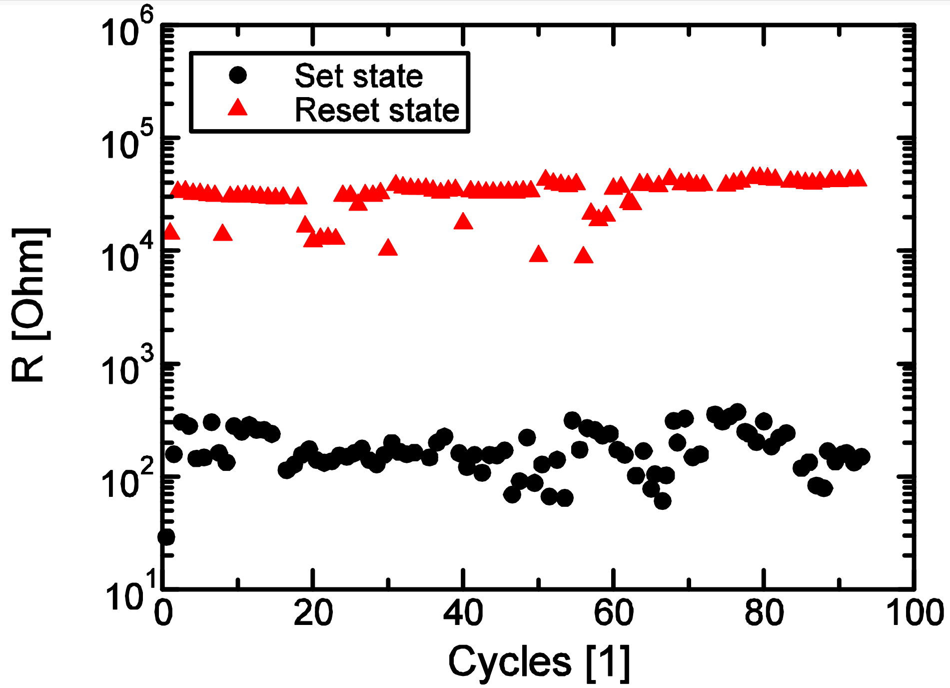
- WP3 – Electrical and reliability characterization
  - Task 3.1 – Device characterization (methodologies, forming, set, reset)
  - Task 3.2 – Compact modeling
  - Task 3.3 – Reliability evaluation (endurance, retention, radiation)
- WP4 – Physical mechanisms, modeling and scaling (operation mechanisms, modeling, degradation mechanisms and reliability, scaling studies)
- WP5 – System design (memory organization, operating conditions, architectural limitations)

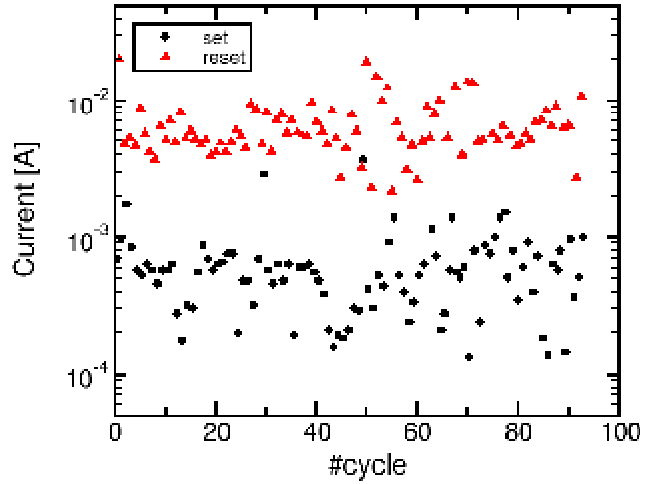
WP3 results: NiO switching

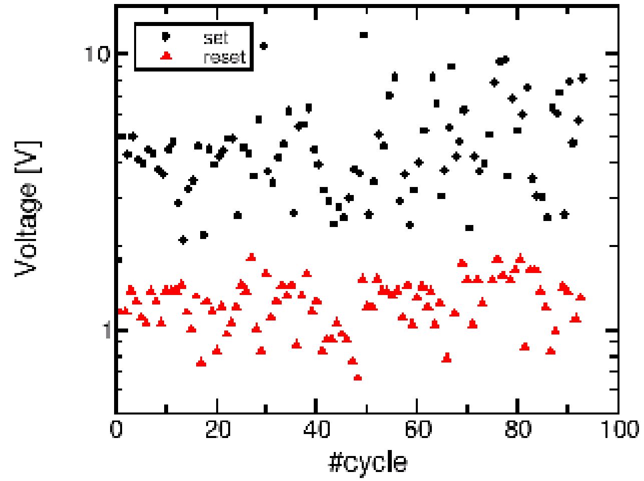




NiO endurance

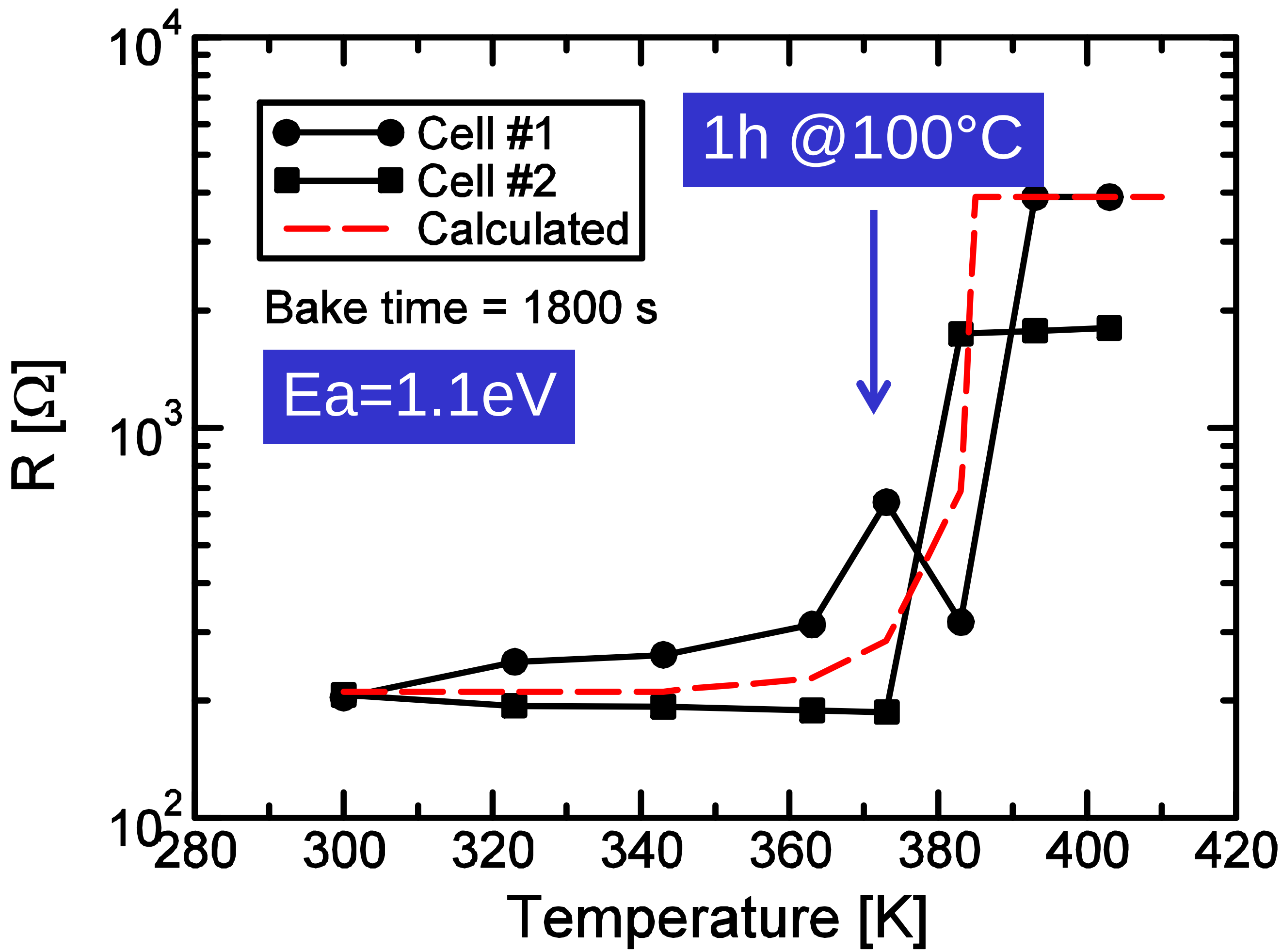






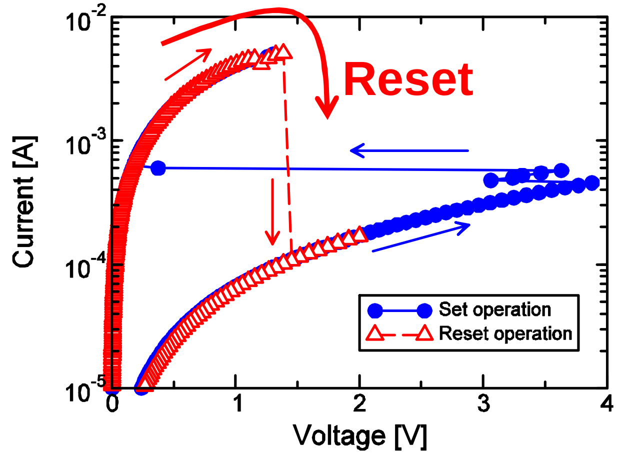
- 100 DC-cycles typically achieved (AC endurance expected much higher)
- Reset current around 5mA (2-20mA)
- Set voltage around 5V (2-12V)

Data retention

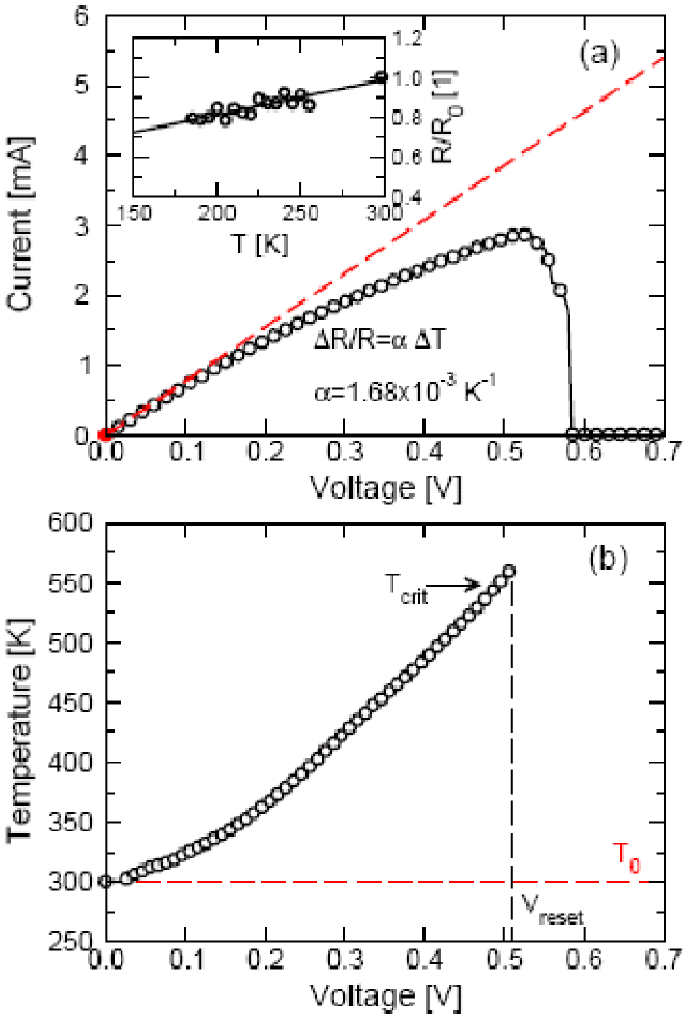


Results in WP4: reset and data loss mechanisms and modeling

- Analysis of the reset mechanism:
  - what is the physics of the reset process?
  - which are the physical parameters controlling the reset current? How to scale down the reset current?
  - Is there a relationship between reset and retention properties?

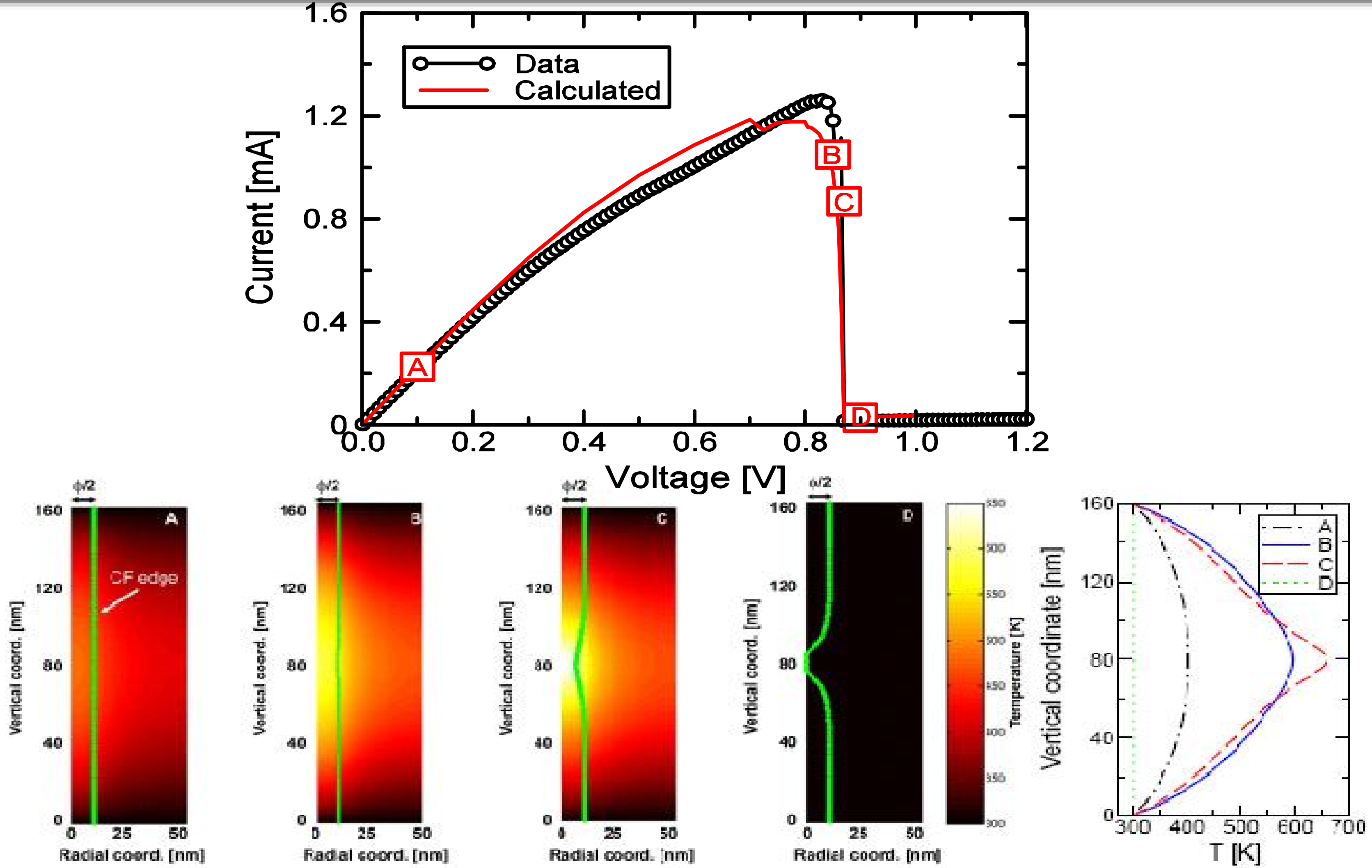


Thermal-dissolution of the conductive filament



1. Metallic filament (ohmic + positive CRT)
2. Heat dissipation + diffusion of conductive species
3. Local, thermally-activated dissolution of the conductive filament

Electro-thermal model for reset



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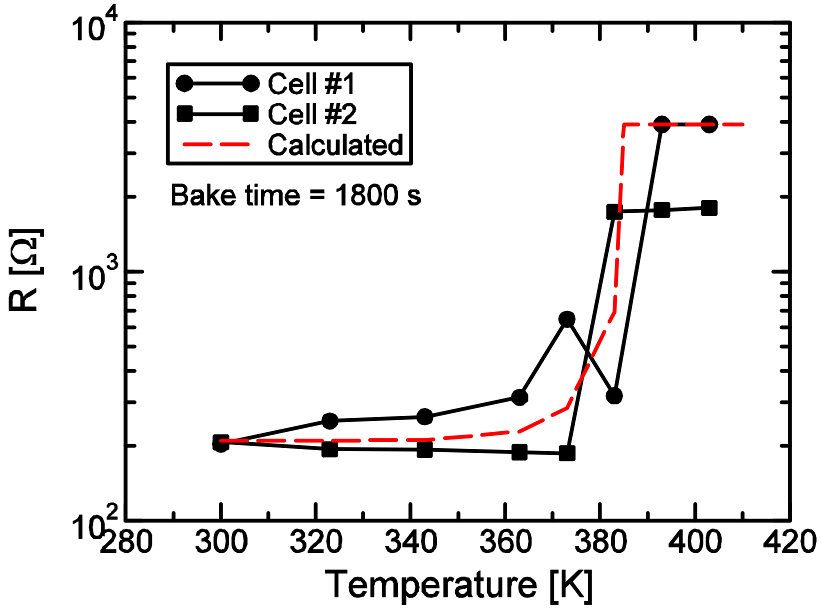
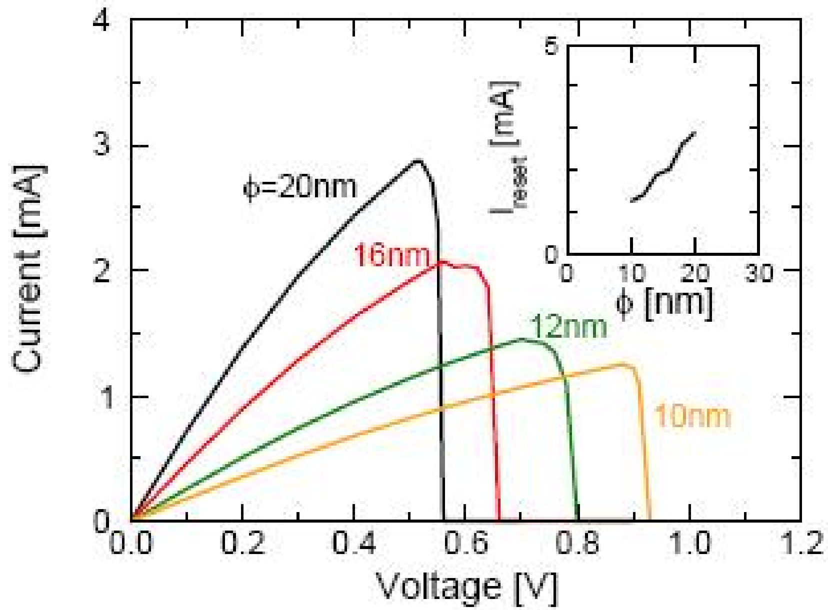
Data retention and reset current scaling





For details see U. Russo, et al., "Conductive filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," IEDM 2007

Summary

- EMMA is a wonderful opportunity for IUNET to express its top scientific profile within a European environment on a new, exciting technology
- NiO-based RRAM displays highlights (unipolar switching, large window $R_{reset}/R_{set}>10$) and lowlights (forming required, retention = 1h at 100°C)
- Reset operation and retention understood, physical model is available
- Outlook:
  - Pulsed operation on analytical cells to benchmark RRAM vs. Flash, PCM, etc.
  - Current scaling and retention requires analysis, modeling and optimization
  - Compact modeling for simulations of memory cells/arrays