Steep Slope Transistors beyond the Tunnel FET concept

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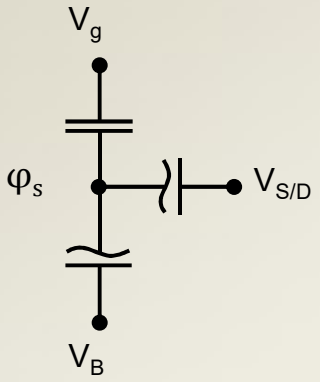
Overcome Boltzmann's Tyranny

Sub-threshold swing may be expressed as

$$S = \frac{\partial V_g}{\partial Log(I_{DS})} = \left[\frac{\partial \varphi_s}{\partial V_G}\right]^{-1}\left(\frac{\partial \varphi_s}{\partial Log(I_{DS})}\right) = \frac{1}{m}\left(\frac{\partial \varphi_s}{\partial Log(I_{DS})}\right)$$

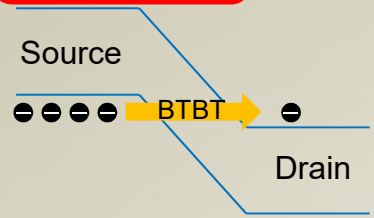


Body factor: $m = \left[\frac{\partial \varphi_s}{\partial V_G}\right]$

In MOSFETs: - second term is limited at 60mV/dec by the thermionic emission;

- *m* corresponds to a paraelectric-capacitance voltage divider → **m ≤ 1**

In TFETs:



- BTB Tunneling, NO therm. emission

→ second term can be < 60mV/dec

- *m* corresponds to a paraelectric-capacitance voltage divider

→ **m ≤ 1**

In NC-FETs: - second term is limited at 60mV/dec by the thermionic emission;

- exploiting **negative capacitances (e.g. FeFET)** → **m > 1**

Outline

Energy filtering at source

- **Super-lattice, steep slope FET (no exper. proof)**

Device concepts *not relying* on energy filtering

- **Negative-capacitance transistors (NC-FETs) based on ferroelectric dielectrics**
- **Piezoelectric FETs (no exper. proof)**
- **Phase change based FETs (Mott transistors)**

Outline

Energy filtering at source

- **Super-lattice based, steep slope FET**

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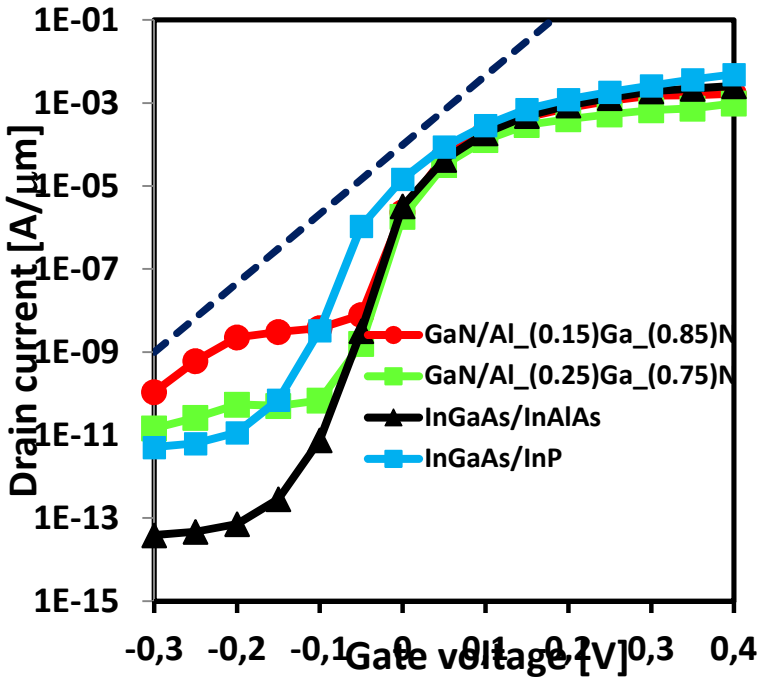
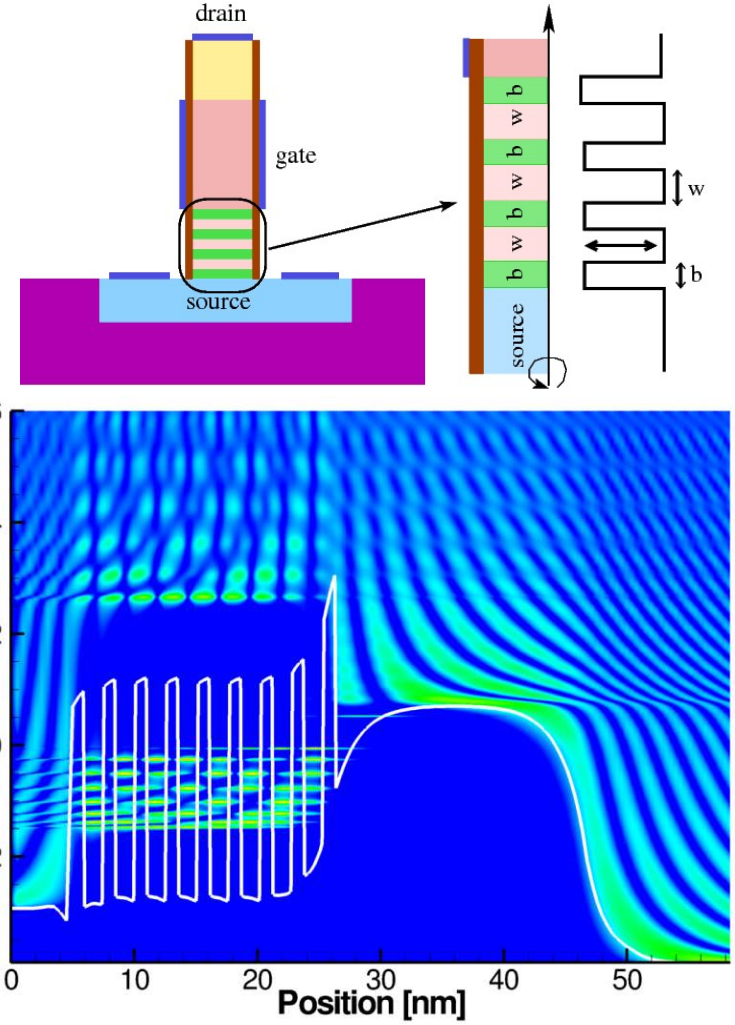
Superlattice based steep slope FET

(P. Maiorano et al., Solid State Electr., Volume 101, November 2014)

To achieve steep slope→ filtering of high-energy electrons





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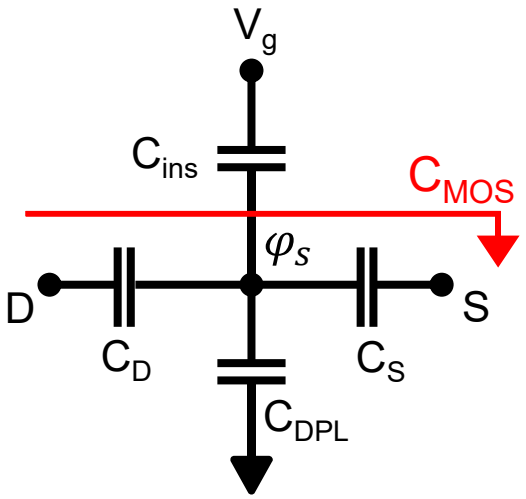
NC-FET concept [S. Salahuddin *et al.*, Nano Letters, 2008]

The **Negative Capacitance** concept can in principle reduce S below 60mV/dec



$$S = \frac{\partial V_g}{\partial Log(I_{DS})} = \left[\frac{1}{m}\right] \left(\frac{\partial \varphi_s}{\partial Log(I_{DS})}\right)$$

$$\Rightarrow \quad m = \left[\frac{\partial \varphi_s}{\partial VG}\right] = \frac{C_{ins}}{C_{ins}+C_{MOS}} < 1$$ **in conventional MOS with** C_{ins} **> 0**

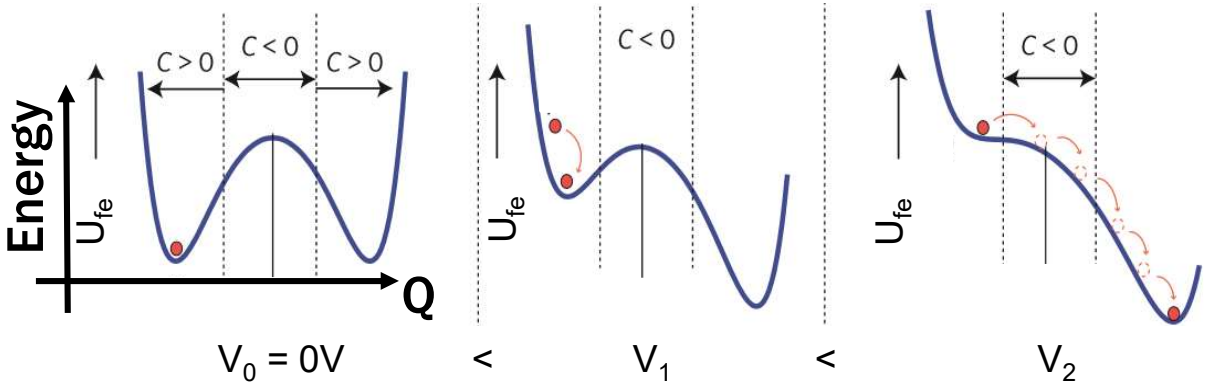
Ferroelectric materials ($BaTiO_3$, Si:HfO_2, Hafnium Zirconium Oxide - HZO) show a negative capacitance $\mathbf{C_{FE}}$ branch, such that charge increases for decreasing voltage:

$$\mathbf{C_{ins} = C_{FE} = - |C_{FE}|}$$

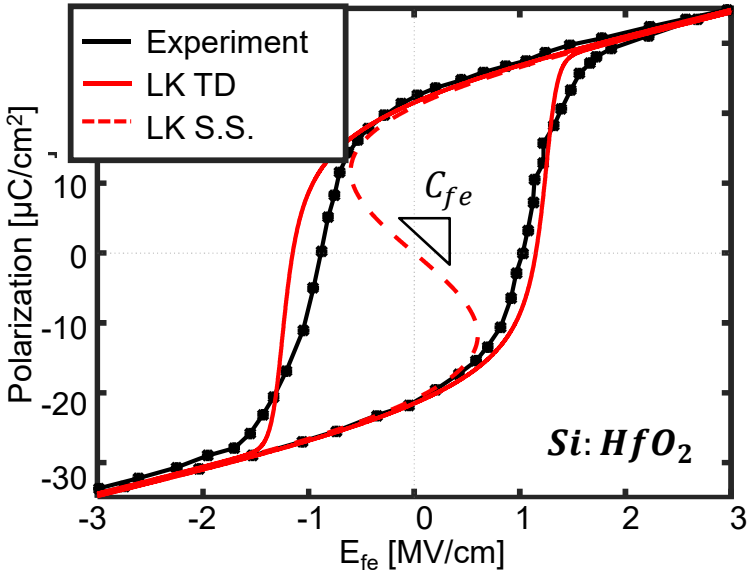
$$m = \frac{|CFE|}{|CFE| - C_{MOS}} > 1 \quad \text{BUT POSITIVE !!} \quad \Rightarrow \quad \mathbf{S < 60\ mV/dec}$$

NC-FET: where does the negative C_{FE} stem from ?

Ferroelectrics are usually described by the Landau-Khalatnikov Equation (LKE):



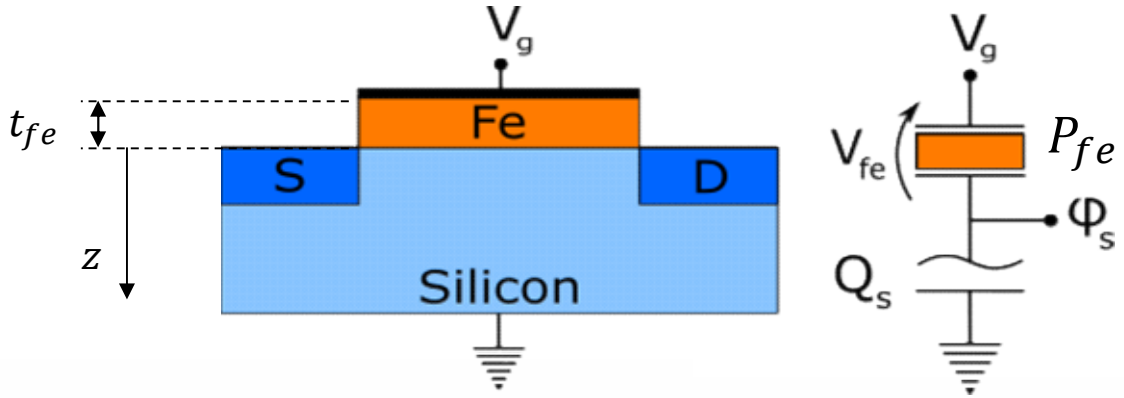
LKE is an Energy-Minimization Approach

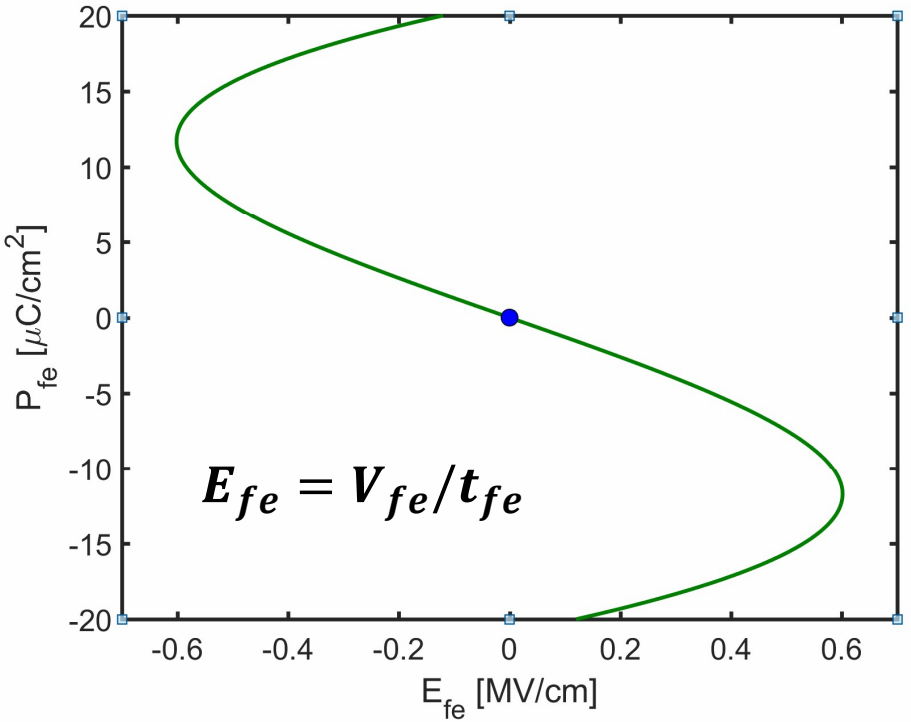


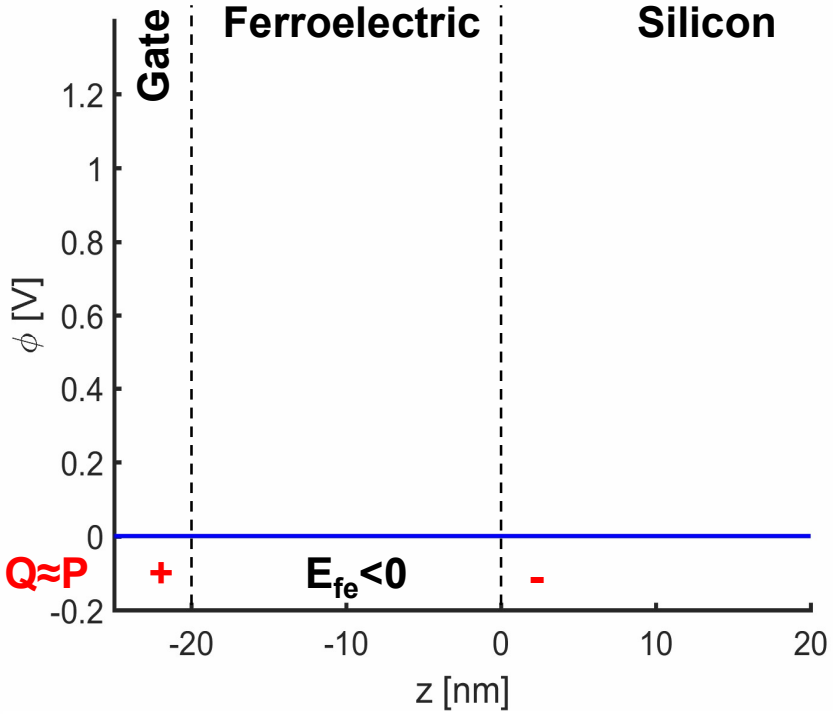
1) Ferroelectric alone is unstable in small E_{FE} region and it has hysteric behavior

2) Ferroelectric with positive capacitance in series should can be stabilized in small E_{FE} region (around E_{FE}=0) and exhibit a negative capacitance behavior $C_{FE} < 0$ [S. Salahuddin *et al.*, Nano Letters, 2008]

Negatve capacitance FETs: voltage gain $\left[\frac{\partial \varphi_s}{\partial VG}\right] > 1$







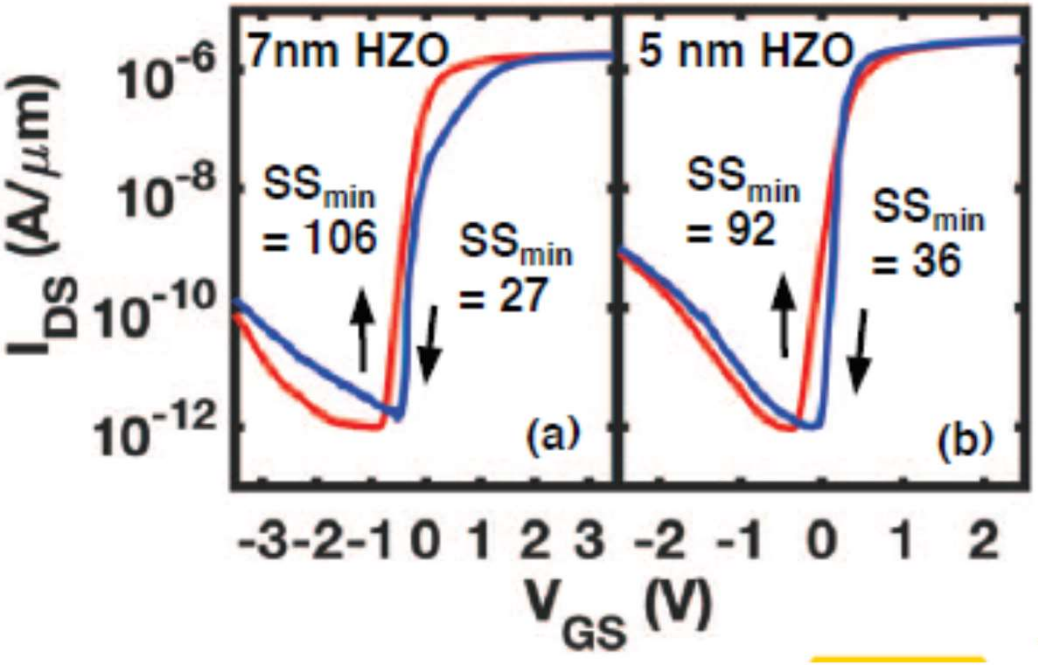
Negatve capacitance FETs

Is there experimental evidence of sub-threshold swing below 60mV/dec in NC-FETs ?

[P.Sharma *et al*., VLSI Symp. 2017]

After P.Sharma *et al.*, VLSI Symp. 2017

Gate last process with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as ferroelectric (FE) dielectric in a metal/ferroelectric/insulator/semiconductor (MFIS) configuration



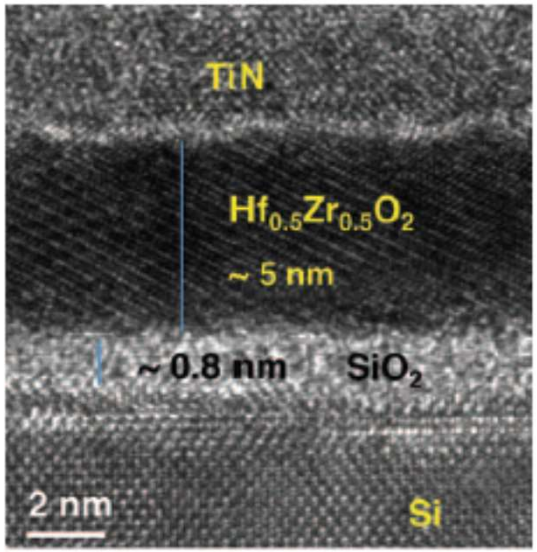


Fig. 2: HRTEM cross-section of MFIS gate stack with 5 nm HZO.

- Long channel FETs (around 2μm)
- Asymmetric and hysteretic I_{DS}-V_{GS} characteristics
- Measurements at low frequency and still too large voltages

Negatve capacitance FETs

IUNET: Possible synergy between *ab initio* analysis of ferro-materials, device-level modelling, circuit exploitation.

Contacts (Udine-Pisa) for the H2020 Call back in April 2017

Europe:

- NamLab (T. Mikolajick), AMO/Aachen (Waser, Lemme), Jülich (Qing-Tai Zhao) Germany
- A.Ionescu at EPFL

U.S.A:

- Berkeley: S.Salahuddin, C.Hu *et al*.
- LEAST Center in Notre Dame: S.Datta *et al*.

Outline

Energy filtering at source

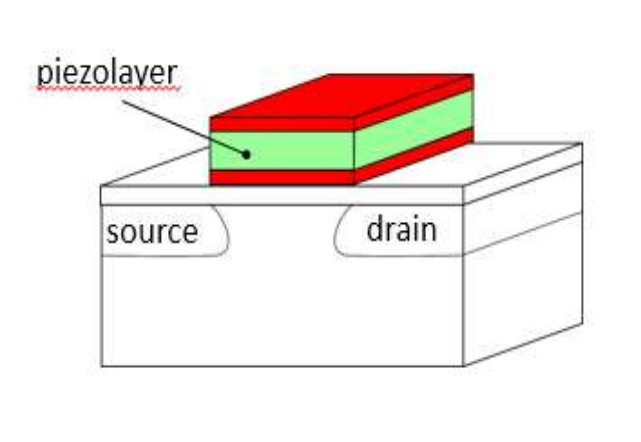
- Super-lattice, small slope FET

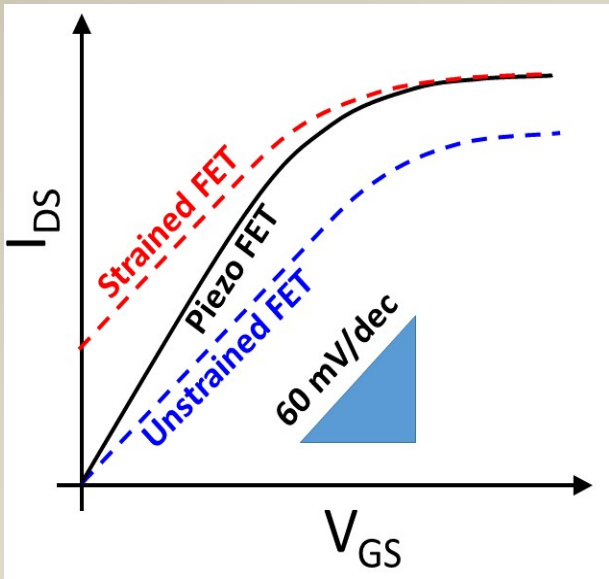
Device concepts *not relying* on energy filtering

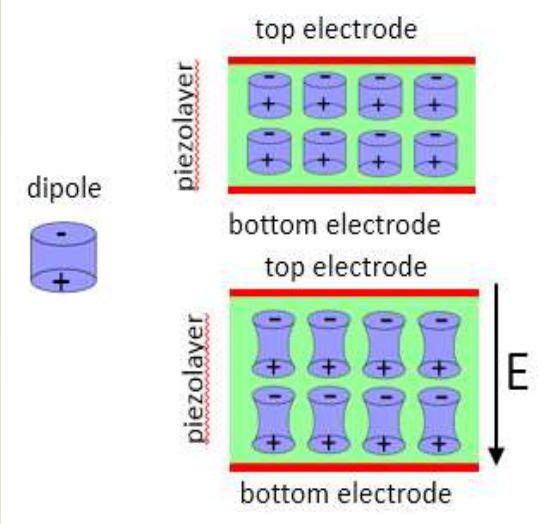
- Negative-capacitance transistors (NC-FETs) based on ferroelectric dielectrics
- Piezoelectric FETs
- Phase change based FETs (Mott transistors)

Piezoelectric FETs – Basic idea

(T. van Hemert, and R. J. E. Hueting, IEEE Trans. on Electr. Dev., pp. 3265, 2013)



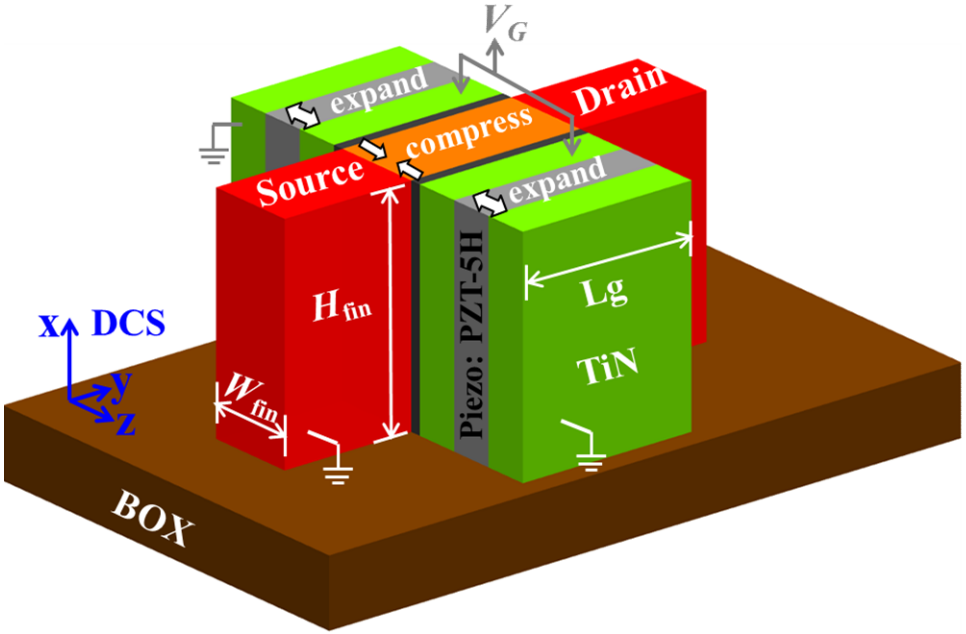


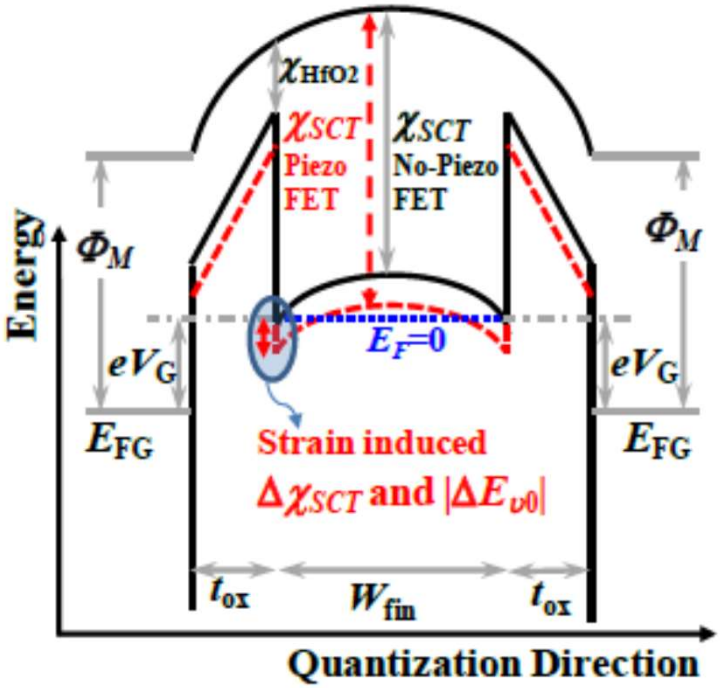


- The converse piezoelectric effect in the piezo-layer is used to enforce a gate controlled strain in the channel material. If the strain is such that the V_T is increased when V_G is reduced (*n*-type FET) and *viceversa*, a sub-V_T swing smaller than 60mV/dec can achieved
- In the turn-on characteristic the transistor effectively switches from an unstrained to a strained I_{DS}-V_{GS} curve

Piezoelectric FETs: possible device architecture

$$T_{ZZ} = \frac{-d_{Z3}V_G}{0.5W_S S_{S,11} + W_{OX} S_{OX,11} + W_G S_{G,11} + W_{PIE} S_{PIE,33}} \quad \text{(Eq.1)}$$





The gate controlled strain in the semiconductor implies a gate controlled electron affinity that results in the simplified SS expression

$$SS = \left[\frac{\partial(\log_{10}(I_D))}{\partial V_G}\right]^{-1} \approx \frac{\ln(10)K_B T}{q}\left[1 + \frac{\partial(\chi_{SCT} - \Phi_M)}{\partial(qV_G)}\right]^{-1}$$

Piezoelectric FETs

Simulations suggest that one can in principle obtain SS values below 60mV/dec but it is necessary to have

1. Large piezoelectric coefficients (d_{z3}) preserved at small piezo thickness
2. Device architectures able to trasfer strain from the piezo to the semiconductor
3. Semiconductor sensitive to strain: large deformation potentials and optimal crystal orientation

Is there experimental evidence of sub-threshold swing below 60mV/dec in Piezo-FETs ?

not to my knowledge

Piezoelectric FETs

IUNET: Possible synergy between *ab initio* analysis of piezo-materials, device-level modelling, circuit exploitation.

Europe:

- R.Hueting at Twente University: contacts with Global Foundries in U.S.A.

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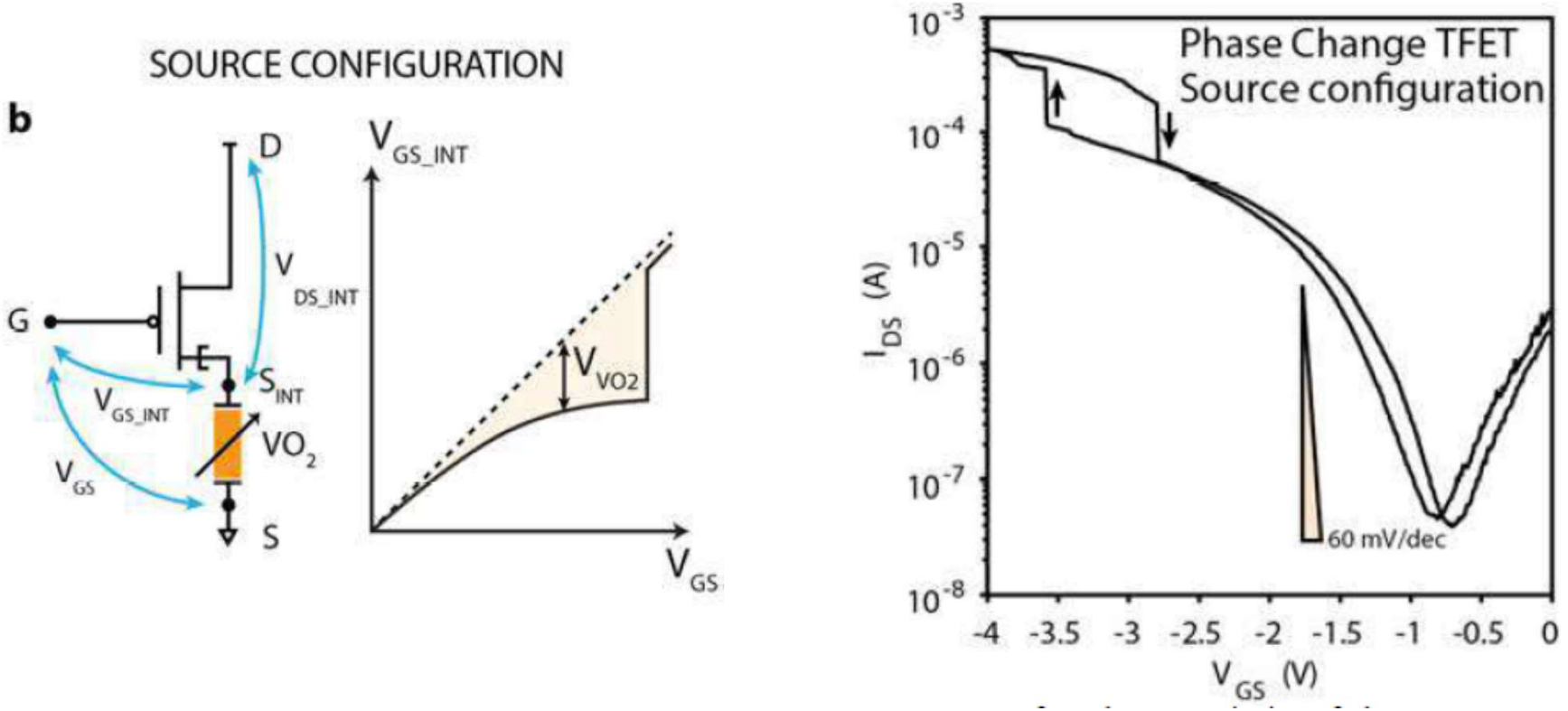
Phase transition based FETs (1)

- Strongly correlated functional oxides exhibit a metal-insulator transition. Vanadium dioxide (VO_2), in particular, exhibits high contrast in conductivity between the two states and the possibility to induce the phase change by electrical excitations
- VO_2-based 2-terminal switches fully investigated [1,2,3]
- VO_2-based 3-terminal devices was attempted in which VO_2 is used as the semiconductor material, but with small transconductance an I_{ON}/I_{OFF} ratio [4,5].

[1] J. Leroy et al., APL, vol. 100, no. 21, p. 213507, 2012.
[2] W. A. Vitale et al., in DRC 2014, pp. 29–30.
[3] W. A. Vitale et al., in IEEE EDL, vol. 36, no. 9, pp. 972–974, Sep. 2015.
[4] D. Ruzmetov et al., J. Appl. Phys., vol. 107, no.11, p. 114516, 2010
[5] N. Shukla et al.," Nature Commun., vol. 6, p. 7812, 2015.

Phase transition based FETs (2): «Hybrid Phase-Change – Tunnel FET (PC-TFET) Switch ....» A:Casu *et al*, IEDM 2016



- Vanadium dioxide (VO_2) is used in series with a FET or a Tunnel FET and results in step-like transitions
- Device concept tightly related to non-volatile type of switching: applications for digital or analog circuits are unclear