Emerging memories: Technology trends and IUNET research contributions

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Outline

- Memory landscape: technology trends
- IUNET projects and research contributions
 - Polimi
 - Unimore
 - Unife
 - Unical
- Conclusions

Memory market and technology

- Strong market concentration
 - NAND (24B\$): Micron, Samsung, Hynyx, Toshiba
 - DRAM (45B\$): Micron, Samsung, Hynyx
 - X-point: not clear market/application now
- DRAM and 2D NAND scaling continues slowly
- 3D NAND more active

DRAM challenges

- Unclear if the vertical DRAM structure can scale beyond 10nm
- Scaling limitations overcame by 3D packaging



Litho, capacitor, metal gate resistivity

Source: J.M Park. Samsuno. IEDM 2015: Chanoveol Lee. Hvnix. IEDM 2015

NAND challenges

- 3D NAND ramps up, as 2D scaling pushes ahead
- Yield and device challenges
 - Poly channel: defect/charge trapping effects on current
 - Thin body
 - Charge trapping



3D Xpoint memory: status

- Technology explored:
 - ReRAM selector is a big issue, and many tech options are currently investigated (OTS, tunneling/Shottky barriers)
 - STT can combine working and NVM strongly reducing the power consumption; suited for IoT



- XPoint™ fills a gap in memory hierarchy, not replacing DRAM nor NAND
- Non-volatile, no active refresh, providing lower standby power than DRAM
- Require significant HW and SW changes

3D Xpoint memory: challenges

- Technology still in the discovery part
- Research needed to find best solutions



Process

- Device (transistor less)
 - Complex physics and variability of storage elements (electron, ionic transport, phase change, thermal, electro-chemical, etc.)
 - Non-linear selectors (varistor or diodes)

- "Novel materials with electrical, structural, and chemical compatibility"
- Integration, e.g., array over logic
- Circuit Simulations
 - Smaller voltage range than NAND
 - Sneak path leakage of large cell array

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Polimi: emerging memories



Polimi: SiO_x-based RRAM devices



- Ti/SiO_x/C RRAM with 1T1R structure, 10⁴ on-off ratio, 10⁸ cycles, 1h @ 260°C retention
- The PCM, STT-RAM and RRAM devices developed/studied in Polimi are currently used for in-memory and neuro-computing projects RESCUE and DEEPEN





Unimore: modeling of RRAM, FeRAM, PCM

- Modeling for novel memories and neuromorphic computing devices
- Structural material changes, ion/vacancy migration, ferroelectric effect, phase change, ... self consistently accounted for multiscale kMC approach
- RRAM, DRAM, FeRAM, selectors



Unimore: RRAM characterization & simulations

1.0

0.9

-sim

oexp

RVF at 1V/s

0

0

- Accurate simulation of device • operations an reliability including statistics
- Noise characterization and • modeling



F. Puglisi et al., IRPS 2015, TED 2015, A. Padovani et al., IMW 2012 - A. Kalatarian et. al., IRPS 2012

UniFE & UniCal: H2020 R²RAM project



Development and design of a radiation hard non-volatile memory technology by using standard CMOS silicon processing.

New R²RAM approach:

Using the Resistive random-access memory (RRAM) technology

www.r2ram.eu

WP #	WP title	Lead Part. short name	PMs	Start month	End month
1	Management	IHP	5	1	24
2	Requirement Analysis and Application Specification	RCD	7	1	6
3	RRAM Technology, Architecture and Cell Development	IHP	23	1	21
4	Design Enablement Platform	IHP	16	1	15
5	1 Mbit Test Vehicle Design	RCD	22	1	20
6	Radiation Testing Campaign	IUNET	46	1	24
7	Dissemination and Exploitation	IUNET	12	4	24
	TOTAL		131		

UniFe: Rad-Hard 1T-1RRAM single device





100

Unife: radiation testing on 1 Mbits RRAM arrays

Two types of radiation:

- high energy (LET=60 MeV/mg/cm2) Xenon ions
- high energy (LET=50 MeV/mg/cm2) proton
- Test Vehicle: 1Mbit RRAM chip
- Before radiation, cells have been formed and programmed in LRS (50%) and HRS (50%)
- After radiation, the chip is still functional and reprogrammable (data through radiation are lost caused by high LET doses)







Unical: micromagnetic simulation framework

Simulation approach to perform a variability-aware analysis of hybrid CMOS/MTJ circuits considering the impact of MTJ and CMOS process variability and the MTJ stochastic switching behavior



R. De Rose et al., "Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework," *IEEE Transactions on Nanotechnology*, vol. 16, no. 2, pp. 160–168, 2017.

Unical: compact macrospin Verilog-A model

 Comprehensive analytical macrospin compact model for perpendicular STT-MTJs including the effects of voltage-dependent PMA, temperature-dependent parameters, Joule heating, MTJ process variations and stochastic switching



R. De Rose *et al.*, "A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs," *IEEE Transactions on Electron Devices*, in press, 2017, DOI: 10.1109/TED.2017.2734967.

Conclusions

- Hottest topics in the "memory" field:
 - DRAM scaling
 - Reliable solution for selectors for x-point
 - Embedded for automotive?
- IUNET active in all emerging memory fields for xpoint: RRAM, PCM, STT-MTJ, FeRAM
- Issue: leading industries far from Europe (Micron, Samsung, Hynyx, Toshiba/Sandisk): access to funding complex
- Opportunity: work on embedded for automotive and smart power applications? Connection to EU industry for projects?