Giornata IU.NET
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Galliun Nitride power devices: status, challenges and future opportunities.

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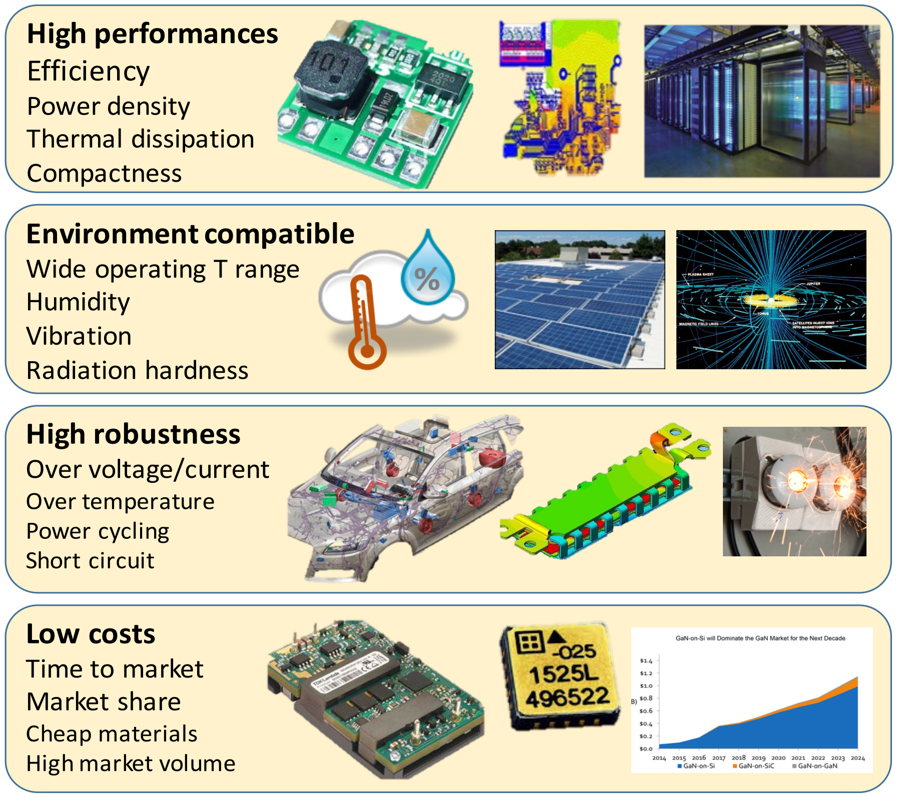
Why GaN-based devices

ECPE Position Paper: Today already 40% of the world wide used energy is provided by electric power. It is expected that this share is going to rise to about 60% until 2040. **This enormous amount of energy not only needs to be produced environmentally friendly, but it also should be distributed and used efficiently**.

Challenging Requirements of Power Electronics



Wide Bandgap Semiconductors (WBG) such as **SiC, GaN, AIN and diamond** show superior material properties compared to Silicon. Due to these unique characteristics (high maximum current, high breakdown voltage, and high switching frequency), these WBG represent the unique material of choice to help solving the energy problems of the future.

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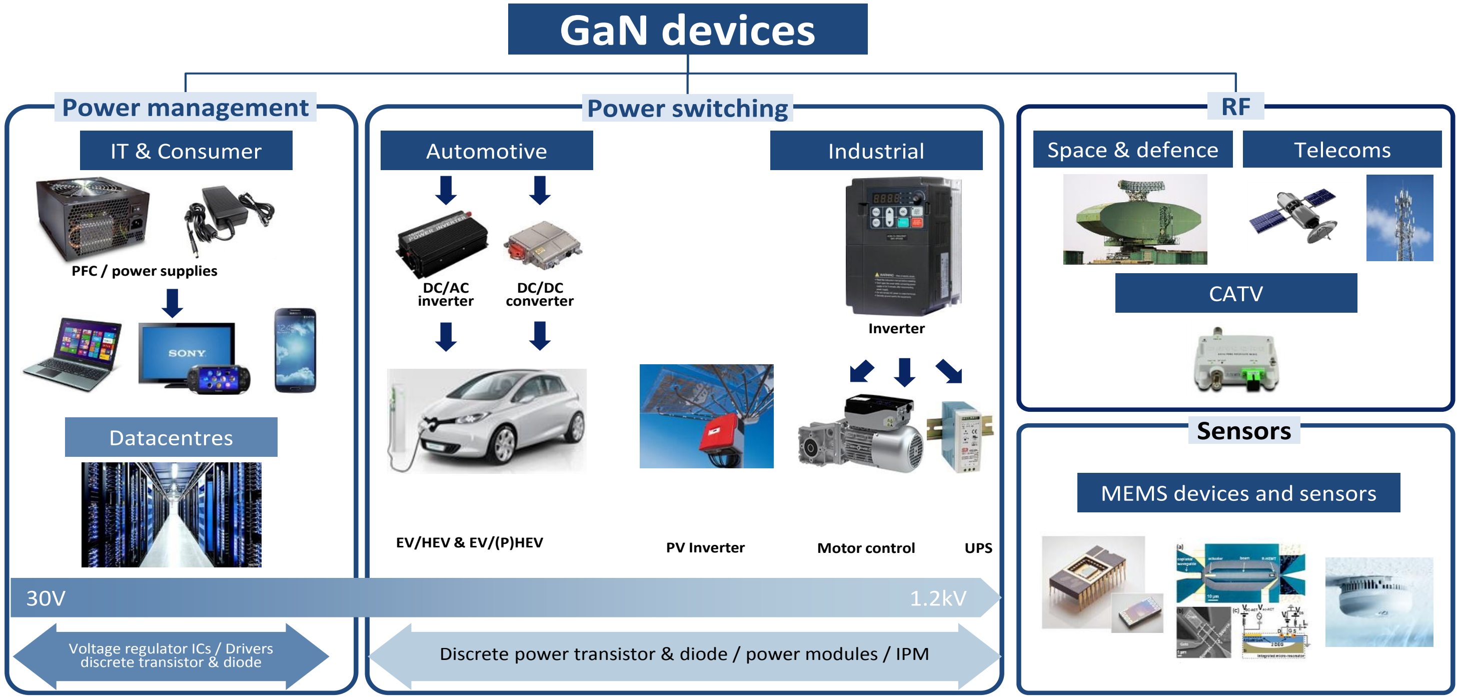
Opportunities of GaN technology



Energy saving is clearly stated in the **SET-PLAN document** . Over 50% of all consumed energy in the world is electrical, and about 60% of all electrical energy is lost due to the many (inefficient) conversion steps (AC do DC, different voltage levels) which are required to bring the electricity from its source to the consumer. Semiconductor devices in general can greatly help to increase the efficiency of the power converters. **The adoption of WBG materials in power electronics is a key factor to reach higher energy efficiency and reducing power management losses**.

http://ec.europa.eu/energy/en/topics/technology-and-innovation/strategic-energy-technology-plan

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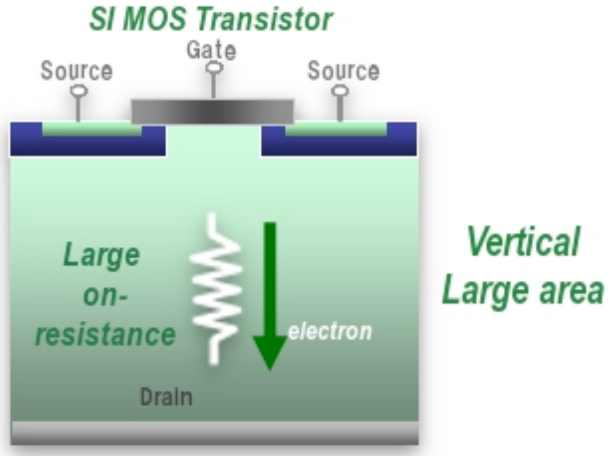
Why GaN-based devices

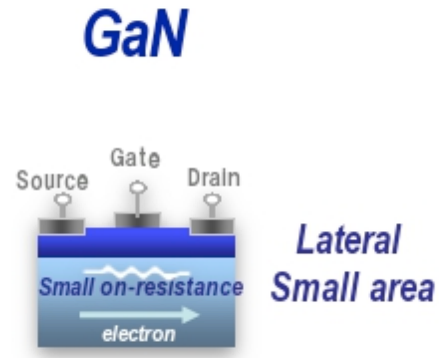
GaN devices offer five key characteristics:

- high dielectric strength,
- high operating temperature,
- high current density,
- high speed switching
- low on-resistance.



Technical advantages of GaN-Based electronics:

- Higher efficiency;
- Reduced heat sink requirements
- 80% reduction in system volume and weight
- Lower voltage drop for unipolar devices
- Increased output power
- Improved transient characteristics and switching speed
- Reduced electrical noise from smaller system packages
- Reduced electrical noise due to virtually zero recovery charge



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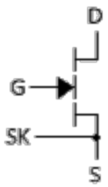
Opportunities of GaN technology

What?

- **100V and 600V** Enhancement (E) mode GaN HEMT
- Single chip, **normOFF** transistor
- Robust, **reliable P-Gate concept**

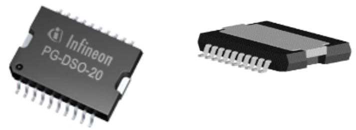


P-Gate
Enhancement mode
GaN HEMT

- **Fastest** normOFF concept available
- Can be tailored for high efficiency or high frequency operation
- Key for **integration** at chip and/or package level

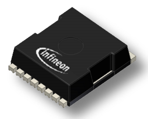
How?

- EMode **600V**, **DSO-20**: sampling prototypes with NDA



Bottom/Top side Cooling

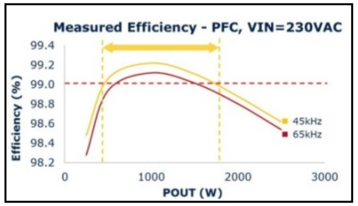
- Emode **600V**, **TOLL**: sampling prototypes with NDA



Low profile, small footprint

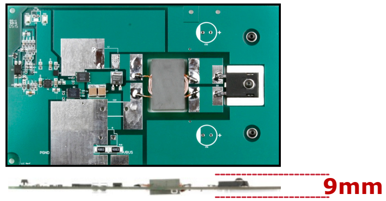
Why?

- **Efficiency**: very high efficient SMPS



Highest efficiency PFC

- **Density**: very compact SMPS



Ultra-thin SMPS

Where?

- Example: **>2.5kW SMPS** in where op. cost matters

Data centers

- Example: **OLED TV** or other **200-800W SMPS**

Ultra-thin TV

100V-200V Emode GaN for Efficiency and Density

Courtesy of Steve Stoffels (imec)

Open Issues in GaN: 1) Substrates

Different Type of "GaN wafers"

	GaN Templates	Low Defect GaN templates (ELO)	Freestanding GaN	Engineered Substrate	GaN boule ("Bulk GaN")
Description	10- 250 µm thick GaN layer on a hetero substrate (sapphire, Si)	10- 250 µm thick GaN layer on hetero substrate with low dislocation density areas obtained by ELO	300-500 µm thick GaN layer separated from a mother substrate.	Thin GaN layer from GaN wafer bonded onto a carrier substrate	GaN single crystals sliced into wafers
TD density	7x10^x to 6x10^x	< 1x10^x in low defect areas	1x10^x to 5x10^x Depending on method	Depends on original GaN wafer	1x10^x to 5x10^x Depending on method
Benefits	Relatively low cost, large diameter available (4")	LD manufacturing possible in low TD areas	Low TD, homogenous with some techniques. Up to 4-6" available	Low cost: one GaN wafer can lead to xx-yy engineered wafers.	Very low TD
Drawback	TD density too high for LD and UHB-LED, wafer bow	TD not homogeneous across surface, wafer bow	Cost	Thermo-mechanical performance driven by carrier	Cost, dimensions Availability
Possible Applications	R&D, possible future in HB-LED*	LD, R&D	LD, UHB-LED, HB LED, Power	LD, UHB-LED, HB LED, Power, RF	High performance devices: LD, UHB-LED, Power

State-of-the-art of GaN substrates

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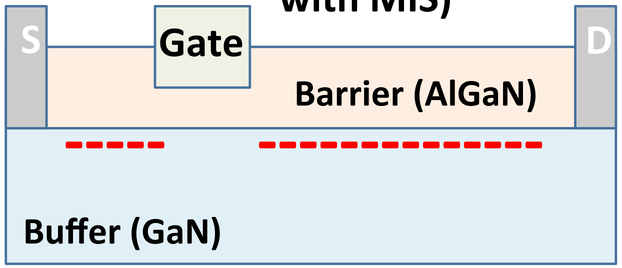
Open Issues in GaN: 2) e-mode

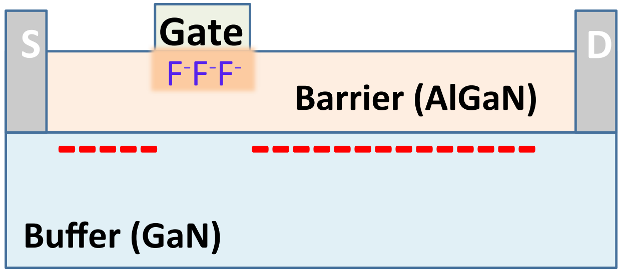
Recess on the Schottky Gate (also with MIS)



- Leakage, trapping, …

Oka et al., IEEE EDL 29, 668 (2008)

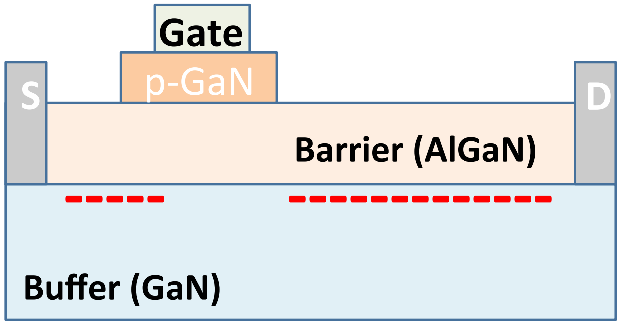
Fluorine implantation



- Vth instabilities, leakage, …

Feng et al., IEEE EDL 31, 2386 (2010)

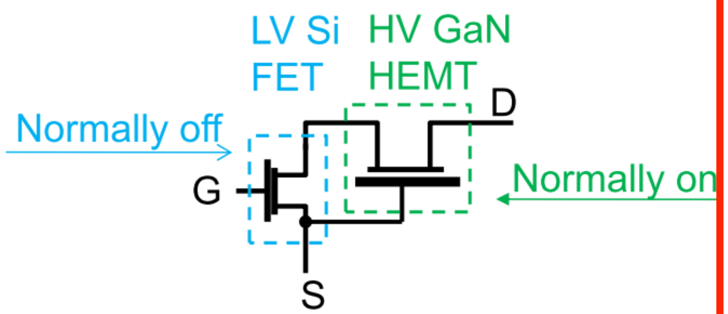
p-type Gate



- Need for p-type, Vth~1.5 V, …

Uemoto et al., IEEE TED 54, 3393 (2007)

Cascode configuration



- Combined Si/GaN, MIS gate, …

Eg. Transphorm, …

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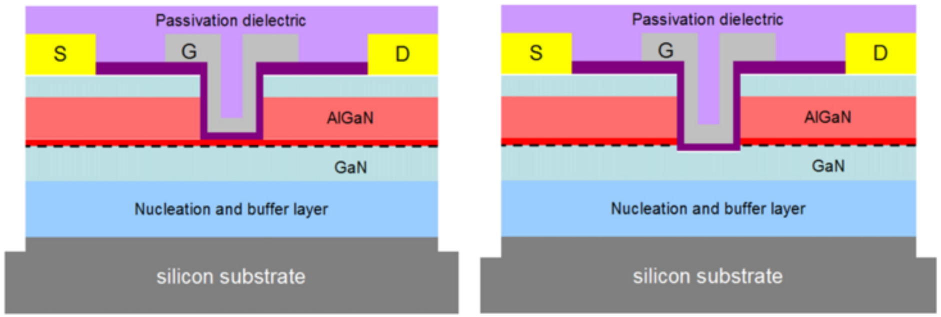
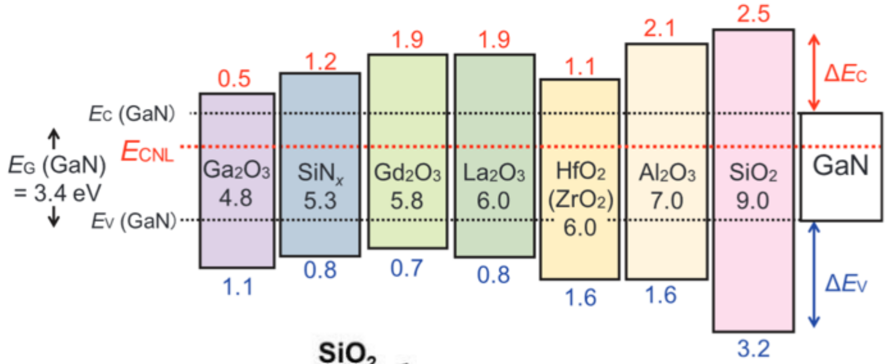
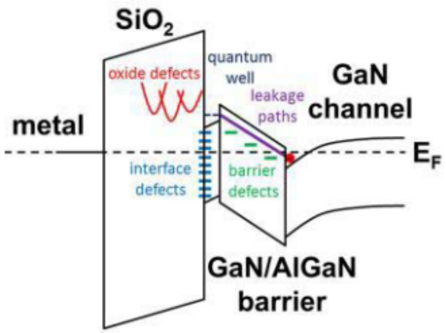
Open Issues in GaN : 3) MIS/MOS

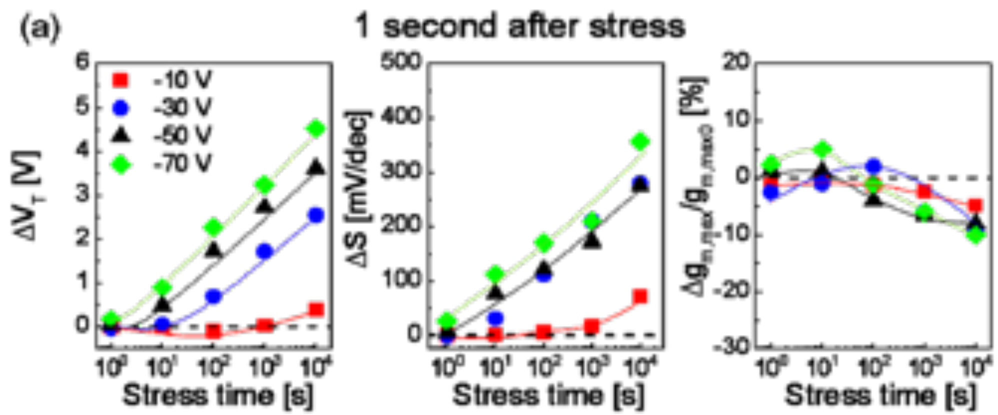


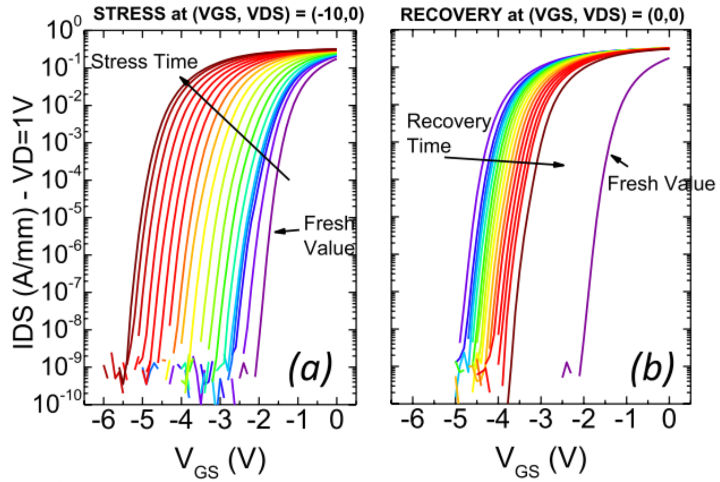




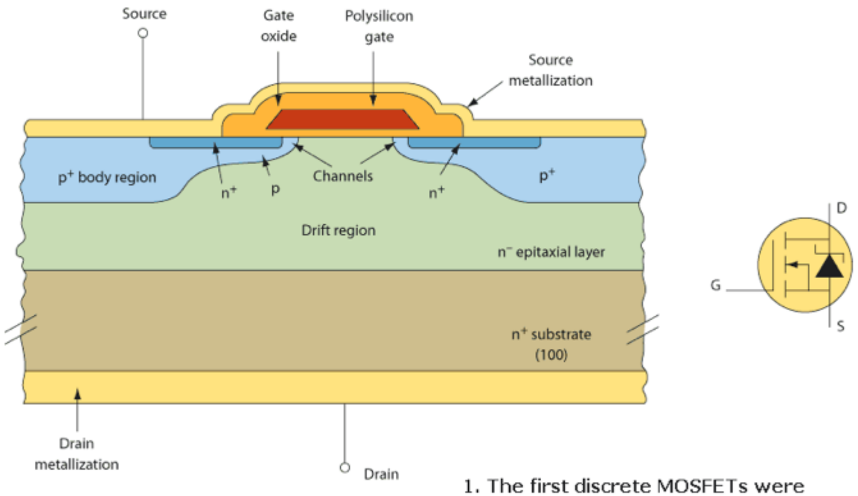
Issues:

- Very complex structure
- Weak e-mode (Vth 1-2 V)
- Traps/defects in bulk and interfaces → Vth instabilities (PBTI, NBTI, …)
- Oxide/Insulator stability (TDDB, ….)

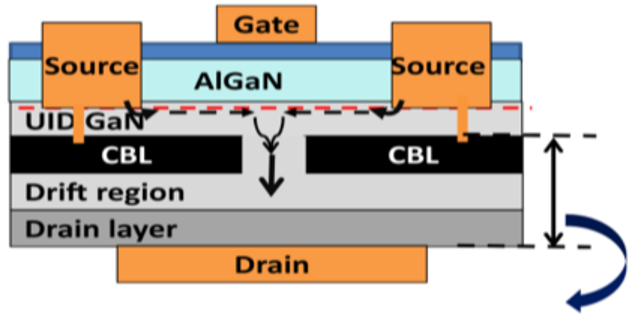




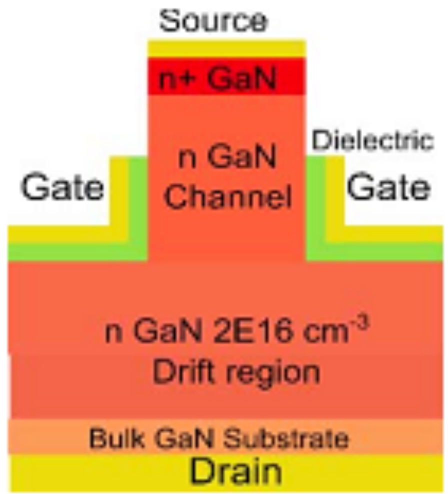
Open Issues in GaN: 4) Vertical



1. The first discrete MOSFETs were made on a completely planar process.



(b) *Blocking voltage is held vertically by depleting the drift region between CBL and drain layer in the off-state*



- All Si power devices are Vertical
- Is this mandatory also for GaN? (Power community want them)
- **Need very good bulk GaN supplier!!**
- If we get out from 2DEG, is GaN still valuable?
- The electrical properties of Bulk-GaN is not far from the SiC, then why GaN?
- The best compromise today is the vertical Fin (proposed by Palacios, MIT)

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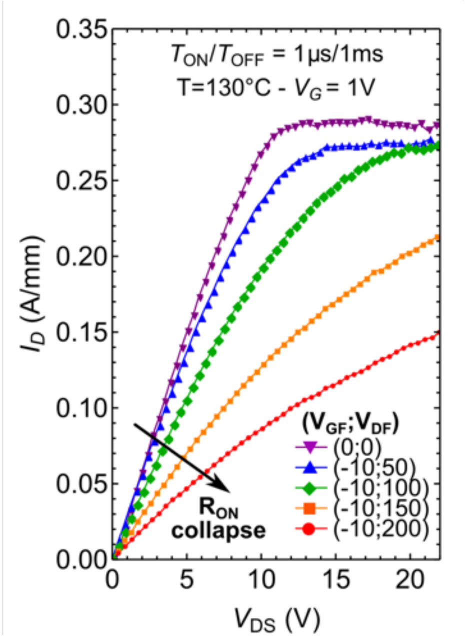
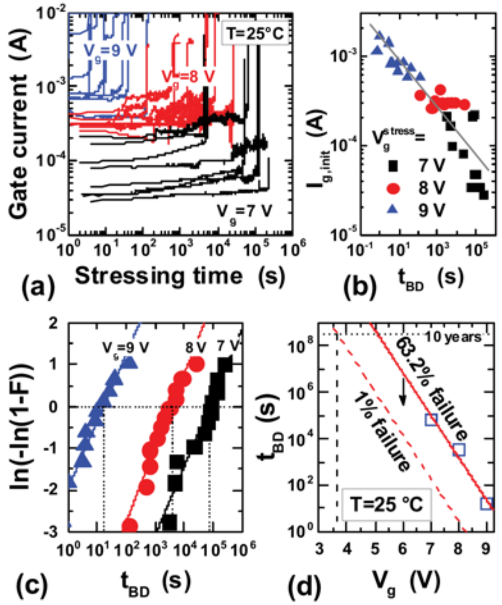
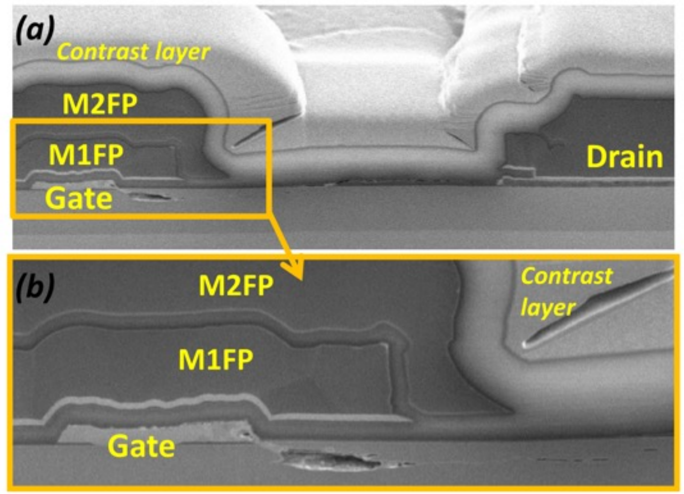
Open Issues in GaN: 5) Parasitic & Reliability







Today's major issues:

- Trapping phenomena; mainly determined by the substrate (C, Fe compensation)
- Degradation (Failure) modes and mechanisms, not fully understood
  - MIS/MOS → TDDB and Vth instability
  - p-GaN gate → max positive gate bias
  - The D-Mode devices (with Thin insulating layer at GaN) have demonstrated good reliability, but the cascode solution is not wanted;
- The qualification procedure has not been yet standardize (large effort in the GaN community)
-

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IU.NET in GaN Projects

E2COGaN targeted the demonstration of **GaN-on-Si as a disruptive high voltage (HV) technology** and High Electron Mobility Transistors through the **whole value chain** up to demonstrators with high industrial, societal and environmental relevance. Aims are **higher efficiency**, **higher switching frequency**, **smaller footprint and weight** and **competitive cost** on system level.

- E2CoGaN (and Hiposwitch) gave a great burst to the European GaN technology development, thanks to the involvement of all major European Players.
- Devices performances and stability greatly improved during the project
- Packaging and demonstrators have also been developed

  - IUNET Contributors:
    - Padova
    - Bologna
    - Modena e Reggio Emilia
    - Calabria

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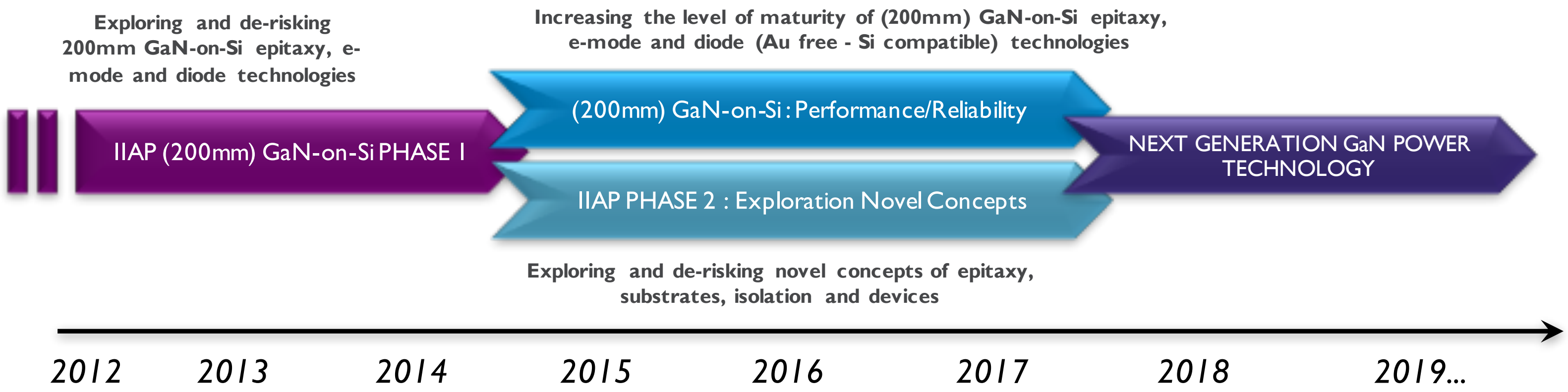
IU.NET in GaN Projects

The H2020 NEREID project is a Coordination and Support Action (n° 685559) entitled "**NanoElectronics Roadmap for Europe: Identification and Dissemination**"

The objective of this project is to elaborate a new **Roadmap for Nanoelectronics** and for the advanced concepts developed by Research Centres and Universities in order to achieve an early identification of promising novel technologies, and cover the R&D needs all along the innovation chain.



IU.NET is involved with UniPD (Gaudenzio Meneghesso)
Task 4.3 Smart Power devices (GaN, SiC ...)

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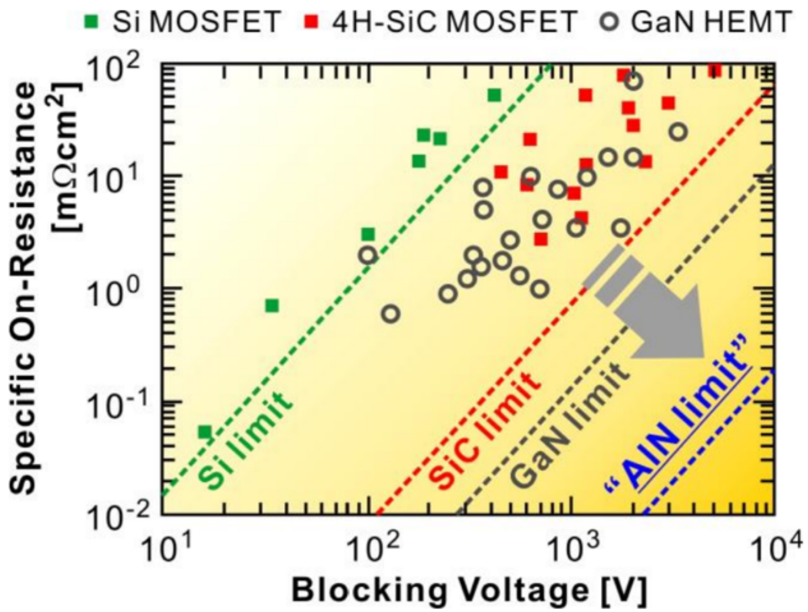
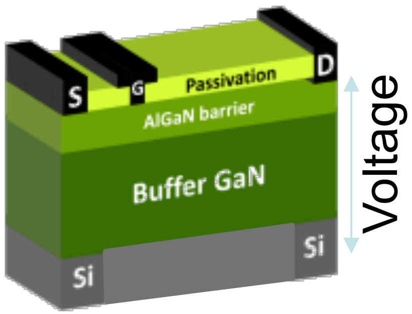
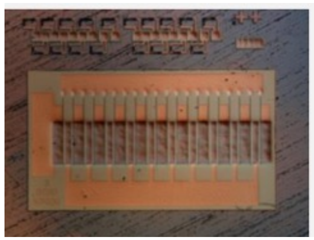
IU.NET in GaN Projects

InRel NPower







- **GaN-on-Si (the current standard)** → The project's baseline technology, with an emphasis on improving reliability by using different epitaxial buffer structures
- **Innovative device architectures** based on substrate removal to increase the maximum operating voltage
- **AlN-based electronics** → Explorative investigation of the epitaxy of Ultra-Wide Bandgap layer structures grown on AlN templates (obtained by HVPE or 3SG) or bulk substrates (grown by PVT)
- Advanced Material Characterization → A major objective is to determine the correlation between material properties and device performance through XRD, AFM, SEM, TEM, CL, PL, EBSD, …

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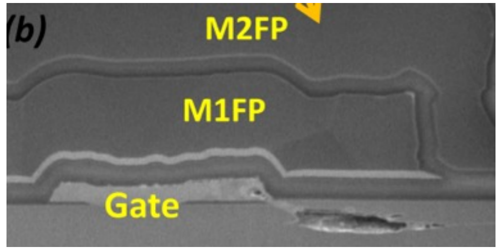
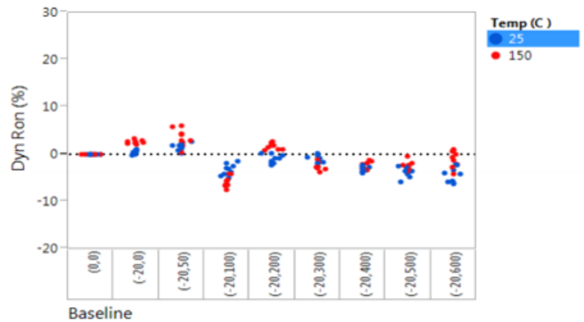
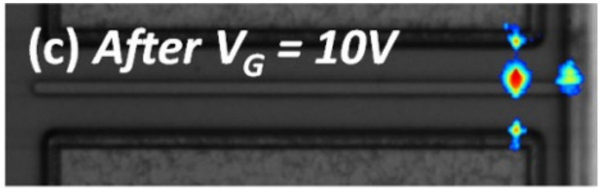
GaN expertiese in IU.NET - UniPD

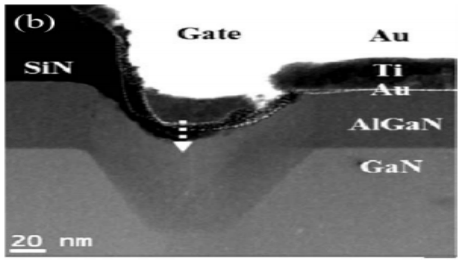
Research topics:

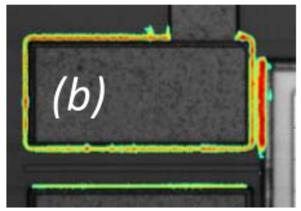
- Reliability of GaN HEMTs with Schottky-gated structure→ Identification of failure mechanisms, analysis of dominant trapping processes
- Charge-trapping issues in 650V GaN MIS-HEMTs for efficient power conversion. Total suppression of dynamic Ron
- Study of the degradation processes of transistors with p-GaN gate submitted to accelerated lifetest
- Study of the reliability of RF transistors for wide band/power transmission based on Ga
- Reliability and stability of vertical GaN-based transistors for power applications
- Time-dependent buffer degradation processes, dependence on epitaxial parameters and device geometry



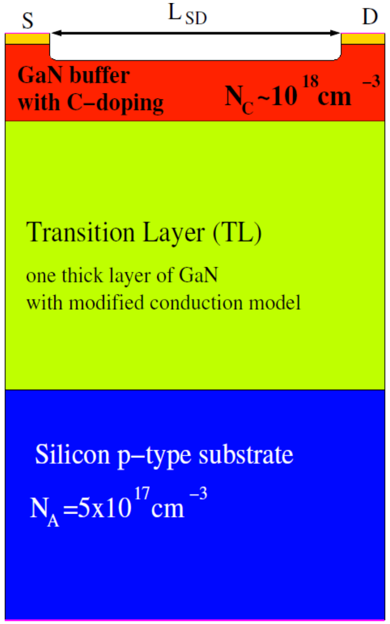








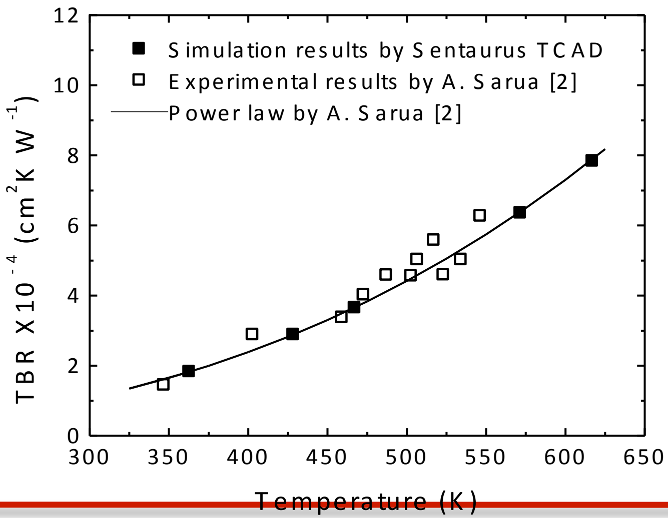
GaN expertiese in IU.NET - UniBO

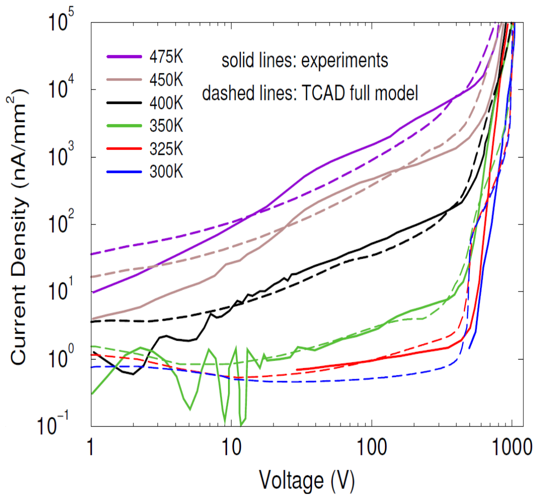


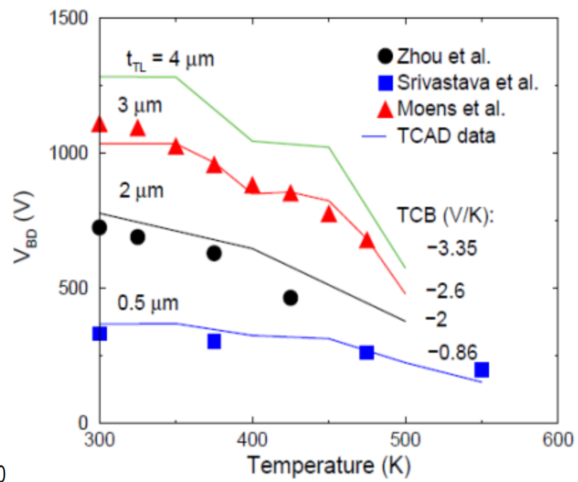
Largely improved TCAD simulation setup:
New impact-ionization model, new approach to account for the role of transition layers and thermal boundary resistance (TBR).

Role of traps in the buffer and at the interface:
TCAD results with traps correlated with experiments on vertical and lateral structures

Explanation of buffer breakdown vs. T:
Electron and hole impact-ionization generation + Poole-Frenkel mobility in the transition layer.







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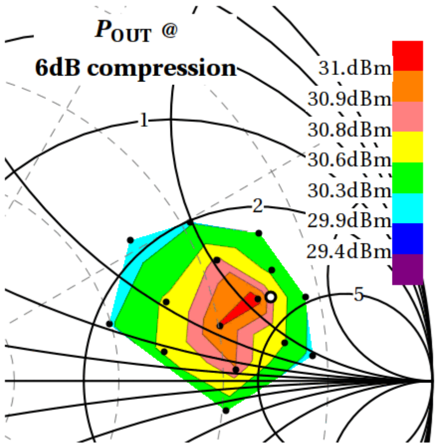
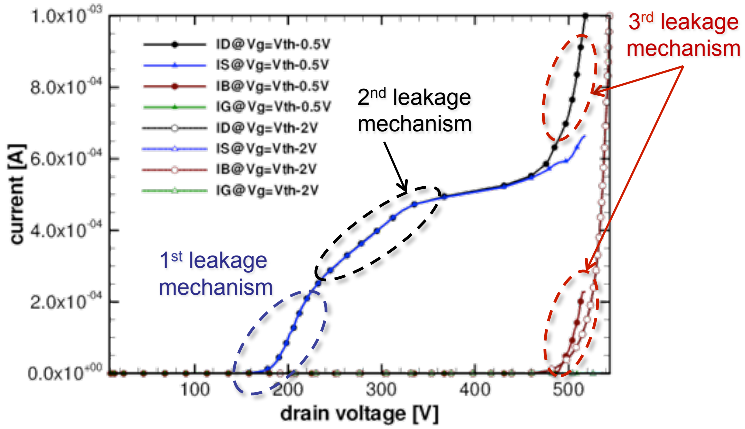
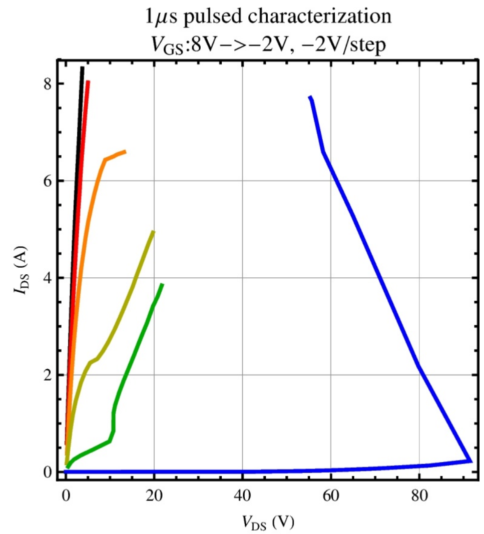
GaN expertiese in IU.NET - UNIMORE

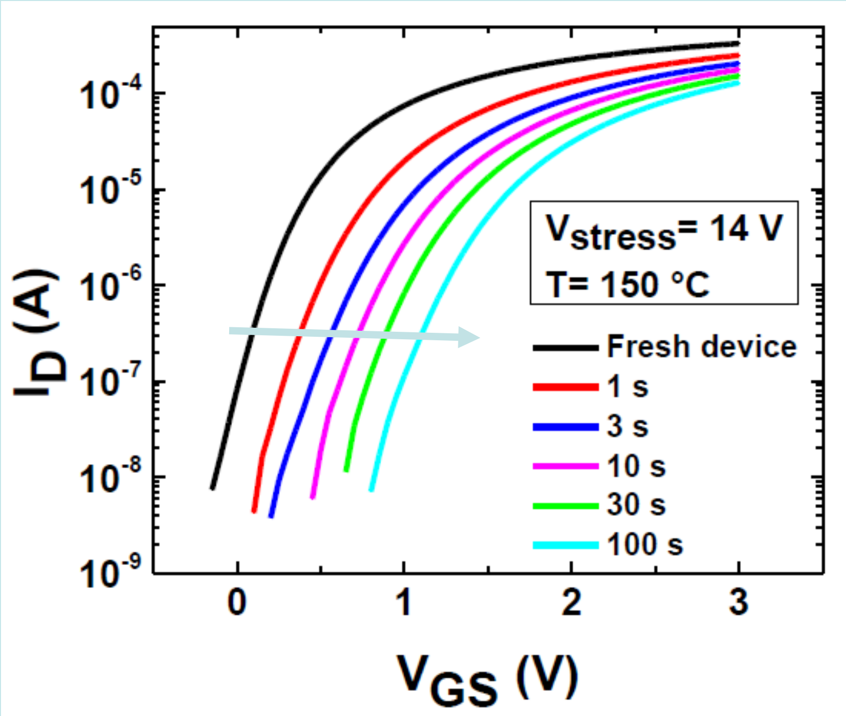
- **Activities:**
  - numerical simulation of trap-related effects, degradation mechanisms, and breakdown effects in GaN HEMTs for RF and power switching applications.
  - numerical simulation of GaN blue LEDs.
- **Recent collaborations/funding:** Univ. Padova, Politecnico di Torino, MIT, Leonardo (Finmeccanica), Infineon, ESA.



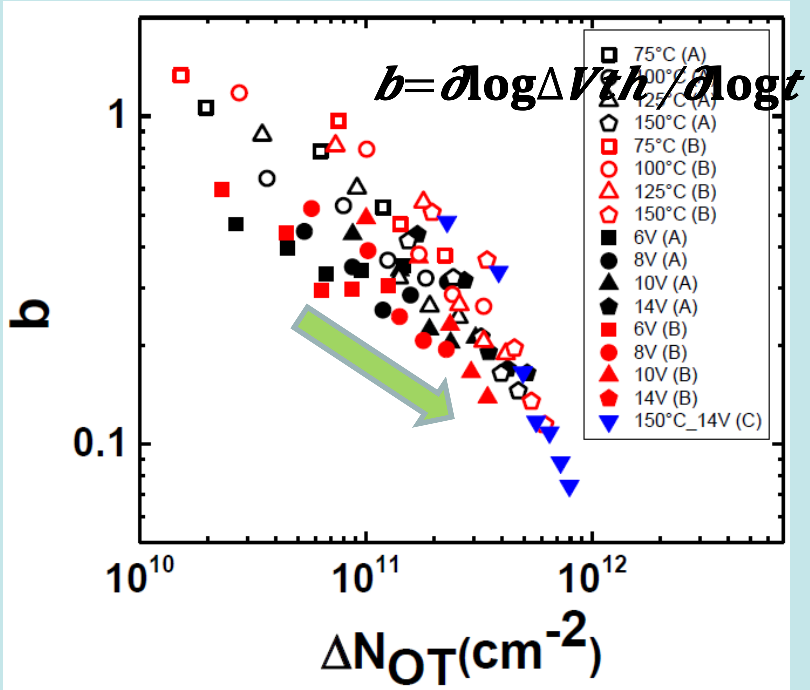




GaN expertiese in IU.NET: UniCAL



PBTI stress ⇒ electron trapping



Trapping rate parameter b versus trapped charges exhibits a universal decreasing behavior independently of stress time, stress voltage, stress temperature, and device-to-device variability

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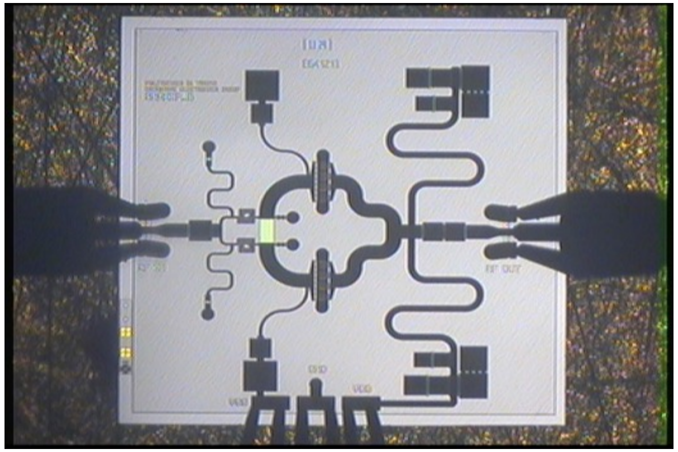
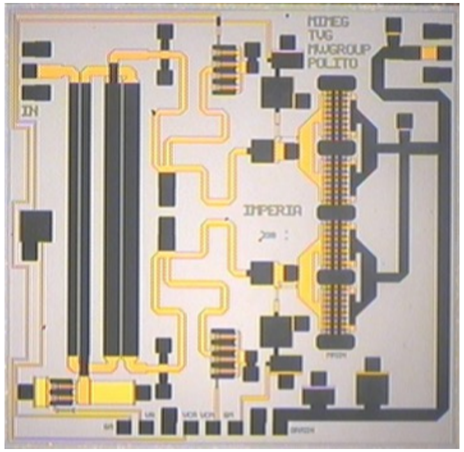
GaN expertiese in IU.NET - PoliTO

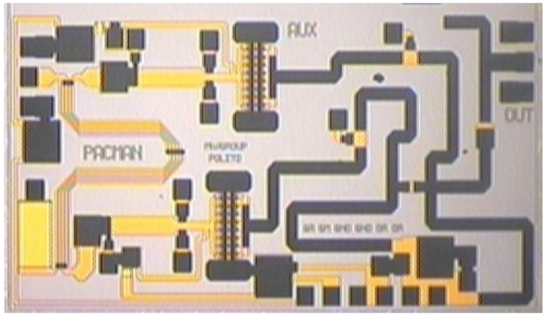
- Characterization and modeling at device level widely exploited for technology assessment (EU KORRIGAN Project) since 2007
- GaN technology investigated with the design of specific demonstrators both hybrid and in MMIC feature with the major research-commercial foundry (Wolfspeed, Qorvo, UMS,OMMIC)
- Design of HPA for Ericsson, Qorvo, Huawei → Backhaul (7-15 GHz) linear and Doherty PAs



7 GHz 5 W linear (class AB)
Power Amplifier
2014



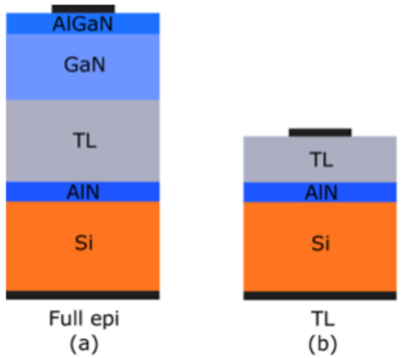
7 GHz 10 W
reconfigurable
Doherty Power Amplifier
2015



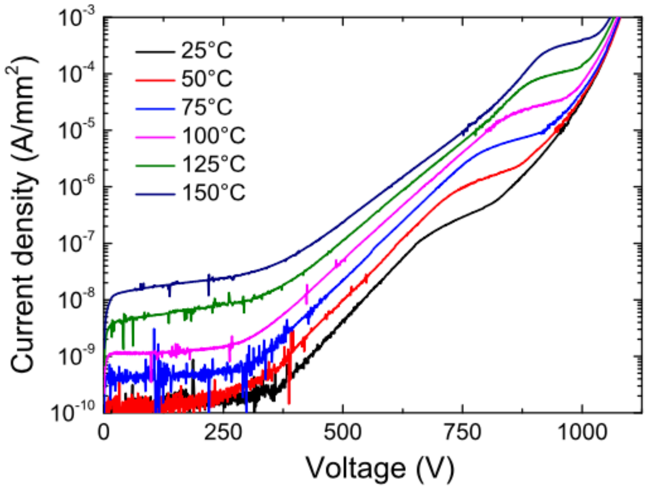
15 GHz 4 W Doherty
Power Amplifier
2016

GaN expertiese in IU.NET - UniPI

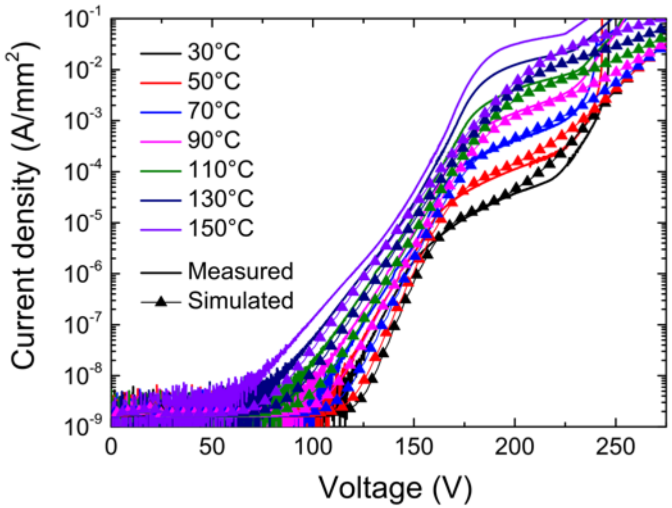
Understanding the substrate leakage current in GaN-on-Si FETs (1 of 2)



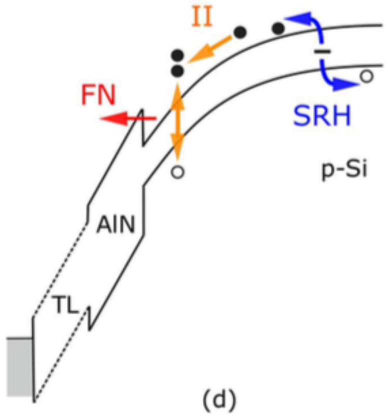
Interrupted runs with only the transition layer (TL) have been fabricated in order to understand the impact of the Si substrate on the leakage current



Leakage current of the Full epi layer



Leakage current of the Transition layer



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