2° MEETING IU.NET
Udine, 10-11 Febbraio 2011

MOdeling and **DE**sign of **R**eliable, process variation-aware **N**anoelectronic devices, circuits and systems

MODERN

ENIAC/CATRENE JTI

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Objective

- The objective of the **MODERN** project is to develop new paradigms in integrated circuit design which will enable the manufacturing of reliable, low cost, low EMI, high-yield complex products using unreliable and variable devices.
- Specifically, the main goals of the project are:
  1. Advanced, yet accurate, models of process variations for nanometer devices, circuits andcomplex architectures.
  2. Effective methods for evaluating the impact of process variations on manufacturability, designreliability and circuit performance.
     - Reliability, noise, EMC/EMI.
     - Timing, power and yield.
  3. Design methods and tools to mitigate or tolerate the effects of process variations on those quantities applicable at the device, circuit and architectural levels.

  Validation of the modeling and design methods and tools on a variety of silicon demonstrators.

Genesi

- 1 call ENIAC 2008
- ENIAC projects: industry driven; Research Institutions are to be connected to industrial partners.
- IU.NET connected to european partners; research activity organized with NXP, ST-F and LETI
- "clustering" of Italian partners
- European approval
- IU.NET re-oraginzed activity according to the needs of Italian industries.
- Mis-matching between European DOW and Italian activity

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Partner del progetto

Participant no. *	Participant organisation name	Part. short name	Country	ENIAC member State	EU Member State/Assoc country
1	STMicroelectronics SA	ST-F	France	Y	Y
2	Austriamicrosystems AG	AMS	Austria	Y	Y
3	Centre Suisse d'Electronique et Microtechnologie	CSEM	Switzerland	N	Y
4	Elastic Clocks S.L.	ELX	Spain	Y	Y
5	TEKLATECH A/S	TEKL	Denmark	Y	Y
6	Infineon Technologies Austria AG	IFXA	Austria	Y	Y
7 not used					
8	IMEP-LAHC Laboratory	IMEP	France	Y	Y
9	STMicroelectronics (Crolles 2) SAS	STF2	France	Y	Y
10	Integrated System Development SA	ISD	Greece	Y	Y
11	Consorzio Nazionale Interuniversitario per la Nanoelettronica	UNET	Italy	Y	Y
12	CEA-LETI	LETI	France	Y	Y
13	Montpellier Laboratory of Computer Science, Robotics and Micro-electronics	LIRM	France	Y	Y
14 not used				Y	Y
15	Numonyx Italy Srl	NMX	Italy	Y	Y
16 (Coordinator)	NXP Semiconductors Netherlands B.V.	NXP	The Netherlands	Y	Y
17 not used					
18	Politecnico di Torino	POLI	Italy	Y	Y
19	STMicroelectronics S.r.l.	ST-I	Italy	Y	Y
20	Synopsys Switzerland LLC	SNPS	Switzerland	N	Y
21	Thales SA	THL	France	Y	Y
22	TIEMPO SAS	TMPO	France	Y	Y
23	Delft University of Technology	TUD	The Netherlands	Y	Y
24	Eindhoven University of Technology	TUE	The Netherlands	Y	Y
25	Graz University of Technology	TUGI	Austria	Y	Y
26	Vienna University of Technology	TUW	Austria	Y	Y
27	Alma Mater Studiorum - Università di Bologna	UNBO	Italy	Y	Y
28	University of Calabria	UNCA	Italy	Y	Y
29	The University of Glasgow	UNGL	United Kingdom	N	Y
30	Sapienza Università di Roma	UNRM	Italy	Y	Y
31	Universitat Politecnica de Catalunya	UPC	Spain	Y	Y

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Costs and funding

Participant n°	Country	Total eligible costs (in €)	Maximum ENIAC contribution (in €)	Maximum national contribution (in €) (where applicable)[1]
1	France	731 711	122 196	97 318
2	Austria	906 594	151 401	226 649
3	Switzerland	551 250	92 059	0
4	Spain	238 000	39 746	126 854
5	Denmark	157 569	26 314	0
6	Austria	1 478 010	246 828	369 502
8	France	327 666	54720	272 946
9	France	1 085 032	181 200	144 309
10	Greece	665 500	111 139	221 612
11	Italy	680 000	113 560	226 440
12	France	1 331 850	222 420	310 323
13	France	374 053	62 467	311 586
15	Italy	960 000	160 320	257 180
16	Netherlands	5 548 950	926 675	1 015 458
18	Italy	1 360 000	227 120	452 880
19	Italy	2 512 000	419 504	623 996
20	Switzerland	432 000	72 144	0
21	France	1 280 338	213 816	170 285
22	France	974 220	162 695	129 571
23	Netherlands	1 255 152	209 610	417 966
24	Netherlands	252 000	42 084	83 916
25	Austria	189 000	31 563	111 510
26	Austria	189 027	31 568	111 526
27	Italy	680 000	113 560	226 440
28	Italy	340 000	56 780	113 220
29	UK	1 488 000	64 128	0
30	Italy	340 000	56 780	113 220
31	Spain	208 200	34 700	173 500
Total		26 536 130	4 247 096	6 308 204

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Partners

- **MODERN** is targeting the transversal Sub-Programme SP7: Design Methods and Tools for Nanoelectronics.
- **MODERN** is a plurality of complementary industrially driven projects for Design Methods and Tools for Nanoelectronics; it will address most of the areas recommended in the ENIAC Annual Work Programme 2008, and in particular:
  - Device, circuit, and system variability and reliability (WP2 and WP3)
  - Hardware/software model driven high-level synthesis/flow/reuse/design. (WP3 and WP4)
- Indicative resources: **206** person-years over 3 years

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Motivation and background

- **Motivation 1: Process Variations**
  - To fully account for the effects of process variation, it is essential: (1) To model process variations for VLSI systems in an accurate, but still efficient way at different levels of abstractions. (2) To devise efficient methodologies to evaluate the impact of variation on various figures of merit, such as timing, power and yield. (3) To adopt design solutions that are able to keep under control the effects of variations on this quantities.
- **Motivation 2: Electro Magnetic Compatibility (EMC)**
  - by creating circuits that are robust with respect to short-term variations, such as those induced by power supply ripple and noise, one may very well reduce the effects of EMI, which are due to periodic sharp waveforms. In MODERN, new design methodologies, along with architectural solutions based on asynchronous and de-synchronization techniques will be defined and developed, in order to provide product designers with an effective approach to reduce EMI, while satisfying the traditional constraints and mitigating the impact of Process Variability, in order to fabricate more reliable and robust electronic systems.
- **Motivation 3: Management of complex systems enabled by new technologies**
  - parallel architectures are an opportunity to work around process variation issues. Industries involved in systems development have experience of complex architectures at both system equipments and system-on-chip levels. This type of experience is applied to applications with either real-time or safety critical constraints.

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Task T2.2: PV-aware device simulation

Focus in this task is on activities to include variability in device simulation tools. TCAD will be used to assess various device architectures in standard CMOS but also in other technologies concerning variability, to identify major sources for variability on simulation level already; process sensitivities will be investigated. New methods will be developed to generate statistical circuit simulation parameter through TCAD, with smart approaches (other than brute force). Furthermore mixed mode device/circuit simulations will be carried out.

…**UNET** will put emphasis on the device simulation of memory cells, transistors for high- performance logic circuits and for low-power mixed-mode applications: At the beginning a methodology will be defined to evaluate the impact of process tolerances and intrinsic variability on the dispersion of electrical parameters with computationally efficient TCAD. Viable modelling approaches to efficiently incorporate new physics phenomena and their fluctuations in future devices will be worked out, taking into account the impact of variations of the dielectric thickness, channel doping and stress conditions. In addition a methodology will be defined to evaluate the impact of PV on a single cell within a memory array. ~~Mixed-mode device/circuit simulation methodologies will be looked into to analyze the impact of fluctuations on the performance of simple digital and analog circuit blocks.~~

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Task T2.3: Electrical characterization of PV, software (TCAD) / hardware comparison & calibration

Basic effects of PV will be characterized based on hardware in different technologies, ranging from mainstream CMOS 45/32nm to new device architectures suitable for 22nm CMOS. Other technologies like NVM or SiC, GaAn/AlGaN power and RF devices will complement the activities. In addition for "non pure digital logic technologies" the devices studied will span over many technology generations, so the PV-methodologies will cover a wide spectrum of devices. In general major sources for PV will be identified and characterized wrt/ further scaling. Variability effects and their sensitivities will be investigated from planar bulk device concepts to new architectures on SOI in 2D or 3D. Device simulation results will be compared to measurements and will be calibrated on hardware data to verify PV methodology and physical understanding of major sources of PV in above technologies. It has to be emphasized that there is a strong link between some activities in WP2.3 and in WP5.1 (silicon demonstration: "test structures for PV analysis"), since test structures and their electrical characterization can be considered as an important step towards demonstration already.

…**UNET** will concentrate on experimental methodologies for characterization of PV on test structures, single cells or simple arrays and on methodologies for evaluation of cell statistics on array performance, for 45 and 32nm planar CMOS and for Non Volatile Memory technologies.

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Task T2.4: Correlation between PV and reliability, reliability modeling

The impact of process variability on existing device reliability degradation models will be clarified. Aging measure- ments will be performed on test structures: Device degradation mechanisms will be identified based on silicon, their effect on PV parameters will be characterized and modeled to allow for a better description of aging during operation.

…**UNET** will work on methodologies to design reliability experiments that allow characterizing the impact of PV on test structures, single cells or simple arrays, on 45nm & 32nm planar CMOS, and on Non-Volatile Memories. It will include the development of compact models including aging effects.

Task T2.5: PV-aware compact modelling

PV and reliability effects have to be implemented in device compact models to be able to accurately describe the impact of variability on circuit operation. Implementation methodologies will be worked out and adopted in standard compact modeling.

…With further scaling it becomes mandatory to come up with viable analytical modeling approaches to efficiently incorporate new physics phenomena and their fluctuations in compact models, including quasi ballistic transport (QTB) features and the impact of variations of the dielectric thickness, channel doping and stress conditions, and with viable compact modeling approaches to reach the best trade-off between accuracy and statistics, including variability. **UNET** will address these aspects involving new physics for 45/32nm CMOS and for non-volatile memory technologies.

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2: PV-aware device simulation		29
inition of a methodology to evaluate the impact of process tolerances intrinsic variability on the dispersion of electrical parameters with a ıputationally efficient TCAD methodology.	PI	5
ble modeling approaches to efficiently incorporate in device ulators new physics phenomena and their fluctuations in future ices, including hole and electron mobility, taking into account the act of variations of the dielectric thickness, channel doping and ss conditions.	UD BO	2 5
inition of a methodology to evaluate the impact of process variability he single cell within a memory array (say RTN: random telegraph se, RDF: random dopant fluctuations).	POLIMI	11
~~elopment of mixed-mode device/circuit simulation methodologies to lyze the impact of fluctuations on the performance of simple digital analog circuit blocks.~~	~~UD~~	4
ırdinamento		*2*

3: Electrical characterization of PV, software (TCAD) / dware comparison & calibration		12
inition of a methodology to design characterization experiments that w characterizing PV on test structures, single cells or simple arrays.	MORE POLIMI	2 3
elopment of Compact Models with emphasis on the trade-off veen "physics based" and "statistics": starting from the selection of ıificant parameters, it will define a methodology to reduce the ıber of parameters.	MORE FE	2 2
inition of a methodology to evaluate cell statistics on array formance.	FE	2
ırdinamento		*1*

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4: Correlation between PV and reliability, reliability modeling	2.	10
inition of a methodology to design reliability experiments that allow racterizing the impact of PV on test structures, single cells or simple ys.	MORE POLIMI	3 3
elopment of Compact Models including aging effect.	MORE	3
rdinamento		*1*
5: PV-aware compact modeling		**15**
ble analytical modeling approaches to efficiently incorporate new sics phenomena and their fluctuations in compact models, including si ballistic transport (QTB) features and the impact of variations of dielectric thickness, channel doping and stress conditions.	UD	2
ble Compact Modeling approaches to reach the best trade-off veen accuracy (nm scaled physics requires a lot of parameters to cribe physical phenomena) and statistics (few significant parameters desirable to catch at best the dispersion of electrical characteristics), uding variability.	MORE FE POLIMI PI	1 1 6 3
rdinamento		*2*

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Task	D	Description	*DUE DATE*	UniBO	UniFE	UniMORE	UniPI	UniUD	PoliMI
T2.2: PV-aware device simulation	D 2.2.2	Device simulation analysis of dominant variability sources in 45nm planar bulk CMOS technologies, and Discrete Power Device, SiC, GaN/AlGaN technologies. Prototype implementation of the treatment of individual dopants and traps in the device modeling tools	12	2			2	1,5	
	D 2.2.3	Device simulation analysis of dominant variability sources in state-of-the-art Non-Volatile-Memory technologies	18						**3**
	D 2.2.4	Forecast of the magnitude of statistical variability in 32nm planar bulk CMOS devices via device simulation. Efficient compact model extraction procedures for modeling process variations and device fluctuations	24	3			**2**		
	D 2.2.5	Application of mixed-mode device-circuit simulations for the analysis of the impact of fluctuations. TCAD based assessment of PV effects of potential 22nm device architectures.	27	2				**4**	
	D 2.2.6	Sensitivity analysis of Non Volatile Memory device performance as a function of individual trap position. Toolbox (methodologies, models, tools) to make dominant variability effects accessible to industrial usage of TCAD, outlook to 16nm device architecture robustness using MASTAR	36			5			**10**
T2.3: Electrical characterization of PV, software (TCAD) / hardware comparison & calibration	D 2.3.1	Characterization of the influence of variability sources in planar bulk CMOS devices down to 45nm. Experimental characterization of Non-Volatile- Memory devices in the presence of PV. Parametric mismatch fluctuation effects in 32 nm FinFETs, first PV results on 22nm FDSOI MOSFETS	12						2
	D 2.3.3	Identification of most relevant process variations in planar bulk CMOS devices down to 32nm, parameter fluctuation effects based on hardware. Sources for PV in new device architectures, suitable for 22nm CMOS; major deltas in comparison to standard planar bulk CMOS	30	1	**3**		1.5		

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T2.4: Correlation between PV and reliability, reliability modeling	D 2.4.2	Hardware results of aging measurements available, on planar bulk CMOS technologies	24						
	D 2.4.3	Implementation of statistical degradation effects into aging models, hardware calibration of degradation effects	33			**3**			2
T2.5: PV-aware compact modeling	D 2.5.1	PV-aware circuit-level models for standard CMOS technologies (down to 45nm), and Non-Volatile-Memory technologies, and Discrete Power Device,SiC, GaN/AlGaN technologies. State-of-the-art based statistical models, based on hardware and/or TCAD.	18		1	**2**			3
	D 2.5.2	Statistical PV-aware models for planar bulk CMOS generation devices (down to 32nm)	30		1				
	D 2.5.3	PV-aware circuit-level models for 45nm analog CMOS technology; Modeling of additional variability sources of 3-dimensional device architectures, for new device architectures for 22nm	33				**2**	2	
TOTALE MESI UOMO (tra parentesi quelli dichiarati e usati per la suddivisione del budget)				8 (10)	5 (5)	10 (10)	7,5 (7,5)	7,5 (7,5)	20 (20)
BUDGET CORRISPONDENTE (€)				56.666,00	28.333,00	56.666,00	42.500,00	42.500,00	113.333,00

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	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
Unità-BO	Implementation of a mobility model accounting for different stress configurations, different crystallographic orientations and ultra-thin body effects in advanced MOSFETs. Sensitivity analysis with respect to uniform variations of doping, stress and oxide/interfacial layer thickness. Application to the analysis of FinFETs.	2	NMX	2.2.2	12
	Sensitivity analysis of Non Volatile Memory device performance as a function of individual trap position. Numerical analysis by means of Sentaurus Device including a PMI model for the electron and hole mobility, incorporating mechanical stress, oxide/interfacial layer thickness and high-k stack effects.	3	NMX	2.2.6	36
	Application of mixed-mode device-circuit simulations for the analysis of the impact of fluctuations.	2		2.2.5	27
	Analysis of new sources for PV in device architectures suitable for 22nm CMOS; major deltas in comparison to standard planar bulk CMOS.	1		2.3.3	30
	Coordinamento	2			
	TOTALE	10			

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Unità-FE	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
	Comprehensive literature overview of statistical modeling and PV aware analysis techniques.	1	NMX	D2.5.1	18
	Evaluation of Hamer and maximum gain routine capabilities and limitations as parameter extraction methodologies. Data analysis tools for statistical studies on main technological parameter variations (oxide thickness, doping and threshold voltage). Usage of BSIM simulations/models for the analysis of PV variations. Experimental analysis of mobility variations as a function of operating conditions and BSIM modeling capabilities. Experimental characterization of temperature effects on mismatch and variations.	3	NMX	D2.3.3 (WP5 D5.1.3 NMX)	30
	Investigations on compact mobility model capabilities to match temperature dependence of parameter variation.	1	NMX	D2.5.2	30
	TOTALE	**5**			

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Unità-MORE	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
	Modelli di correnti di leakage in dielettrici di tunnel e di interpoly (SiO_2, Al_2O_3, stack compositi eventualmente con altri materiali high-k) per memorie a FG	3	NMX	D2.2.6 D2.4.3 D2.5.1	36
	Integrazione in SW commerciale	1	NMX, SYN	D2.2.6	36
	Estensione del modello al punto 1 per materiali memorie charge-trapping	2	NMX	D2.4.3	33
	Modellizzazione di rumore RTN su corrente di GATE su stack diversi (SiO_2, Al_2O_3, HfO_2, stack compositi)	3	NMX	D2.4.3	33
	Compact models of selected aging effects	1	NMX	D2.4.3	33
	TOTALE	**10**			

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Unità-PI	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
	TOTALE	7,5			

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Unità-UD	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
	Models for new physical effects in advanced MOSFETs (Strain)	2	NXP	2.2.2	12
	Fast and efficient models for new physical effects in advanced MOSFETs (quasi ballistic transport)	2	NXP	2.5.2	30
	Mixed mode device-circuit simulation .	0		2.2.5	27
	Modello non-locale di mobilità che tenga conto di droganti/trappole discrete e gate oxide roughness .	2	NMX	2.2.6	36
	Studio effetto di quantizzazione e conduzione non-uniforme (narrow-width, rounding area attiva, ...) su celle con scaling aggressivo tipo FinFlash:	2	NMX	2.2.6	36
	TOTALE	**8**			

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Unità-PoliMI	Attività	Effort	Partner Tecnologico	Deliverable	Due Date
	Caratterizzazione sperimentale PV su memorie Flash	3	NMX	D2.3.1	12
	Benchmarking PV su struttura Flash 3D	3	NMX	D2.2.3	18
	Implementazione modello compatto di PV nella stringa NAND	4	NMX	D2.5.1	18
	Simulazione di effetti PV in memorie Flash scalate	10	NMX	D2.2.6	36
	TOTALE	**20**			

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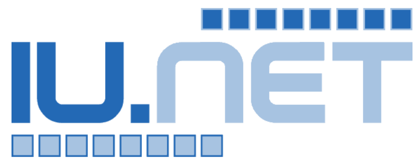

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Important dates:

- 1 march 2009 – beginning
- 3 yrs duration

Deliverables:

- D2.2.2: due at M12 - done
- D2.2.3: due at M18 - done
- D2.2.4: due at M24 – to be done
- D2.4.1: due at M6 - done
- D2.5.1: due at M18 - done
- D6.2.3: due at M18 - done

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Difficoltà tecniche

- problemi legati alla clusterizzazione
- difficoltà legate alla gestione dei template devices
- partner industriale (numonyx-micron) cambia idea e ri-organizza
- pubblicazioni inter-unità e con partner

Difficoltà gestionali

- difficoltà legate alla contrattualistica e al finanziamento (asincronia progetto/contratto; difficoltà di rendicontazione)
- difficoltà di comunicazione interna

Input per progetti futuri

- migliore comprensione del ruolo di IU.NET nel progetto
- chiarire ruolo di coordinatore
- migliorare comunicazione interna
- favorire interazione tra le Unità di IU.NET
- meccanismi di controllo per le Unità