2° MEETING IU.NET

Udine, 10-11 Febbraio 2011

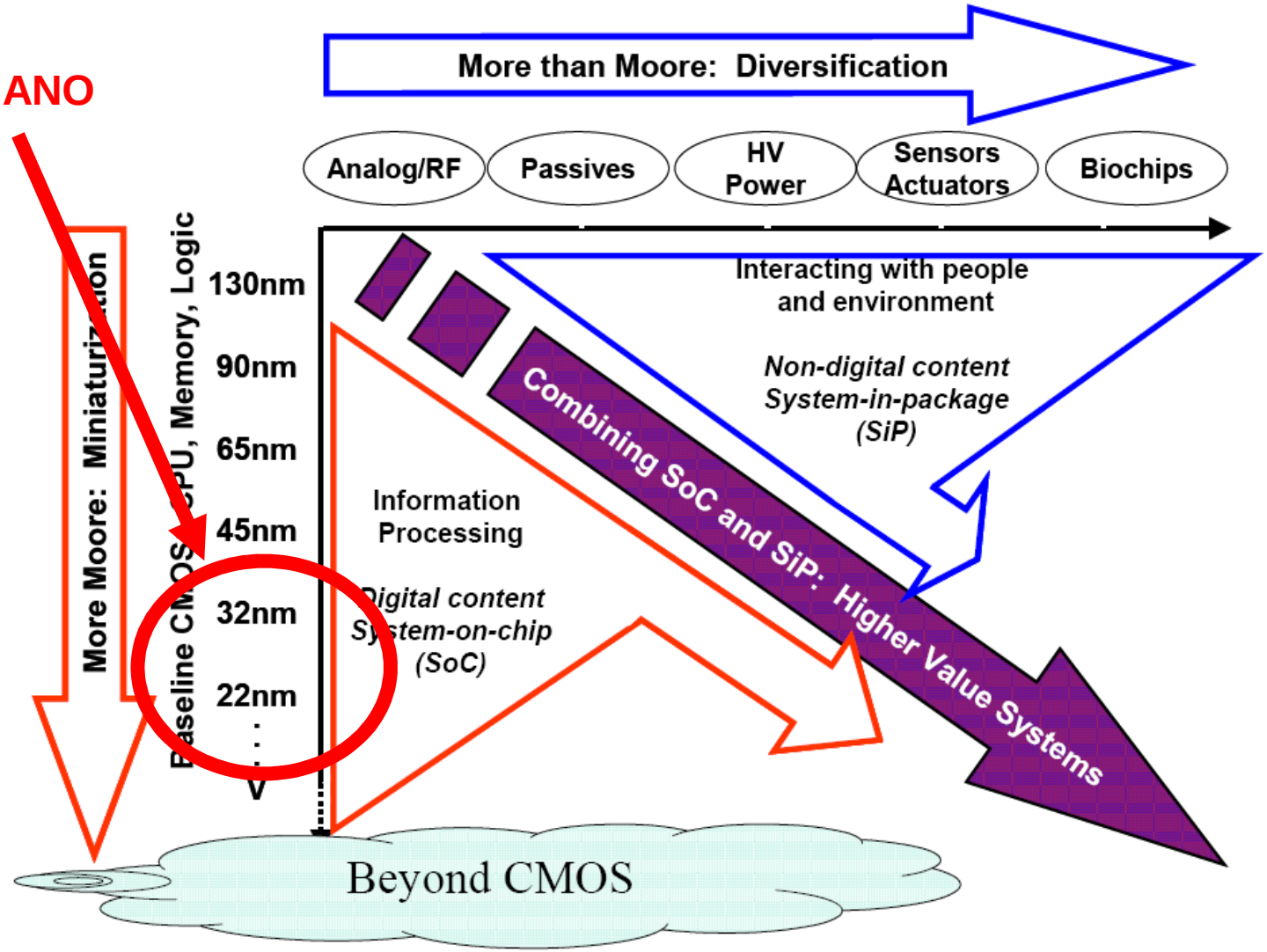
Le Attività di IU.NET nel Progetto PULLNANO

www.pullnano.eu

Luca Selmi

IU.NET- DIEGM - Università di Udine

Scenarios for Nano-Electronics

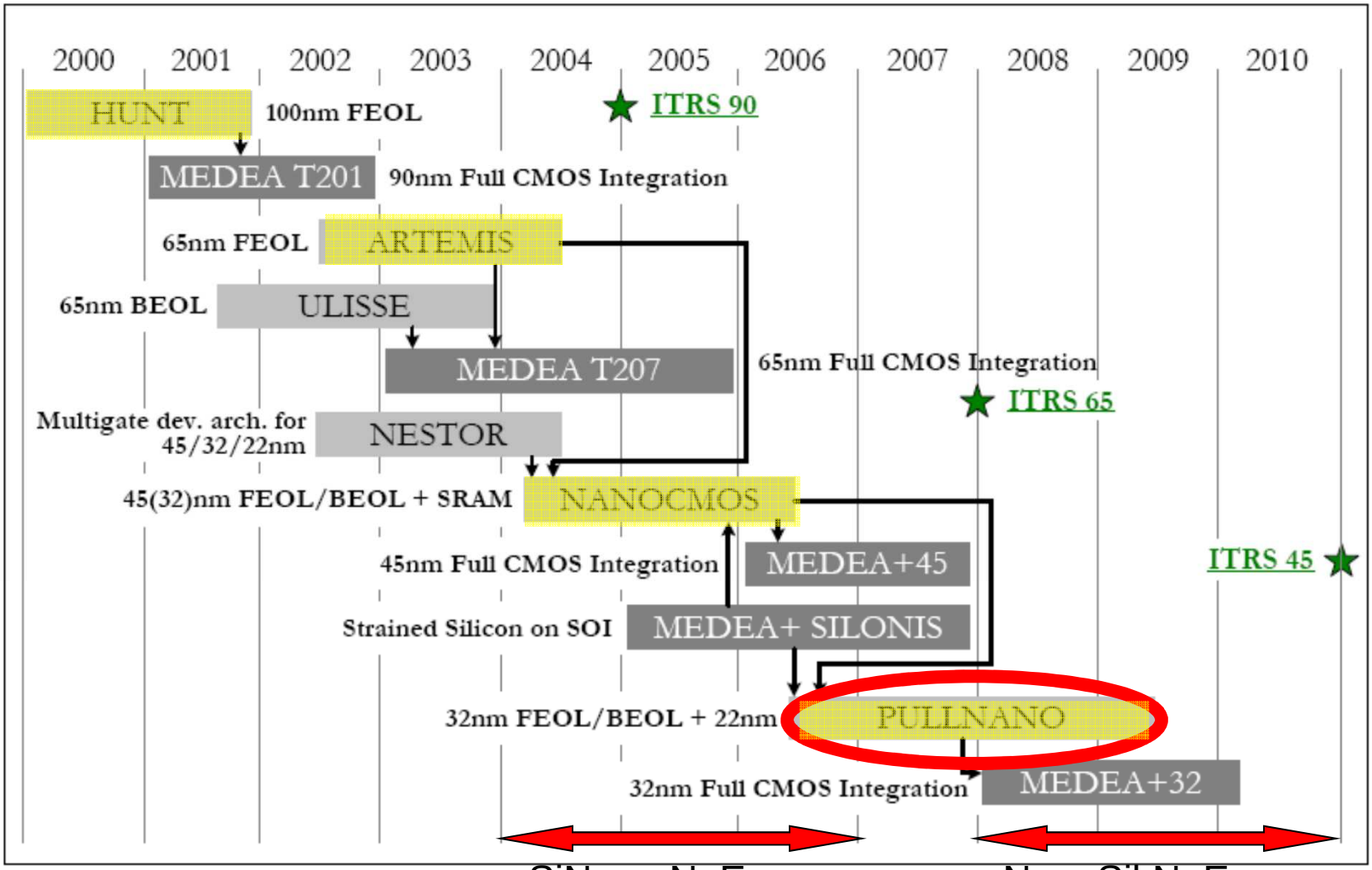


[ITRS, 2005]

PULLNANO Objectives

1. Demonstrate feasibility of 32nm CMOS technology through an SRAM test vehicle (bulk, SOI, FinFET).
2. Prepare the 22nm node in terms of modeling, materials, devices, interconnect scheme, characterization.
3. Boost synergy Technology/Design to cope with power and interconnect delay limitations.
4. To be a forum of European equipment suppliers for the establishment of future tool specifications.

EU projects in Nano-Electronics

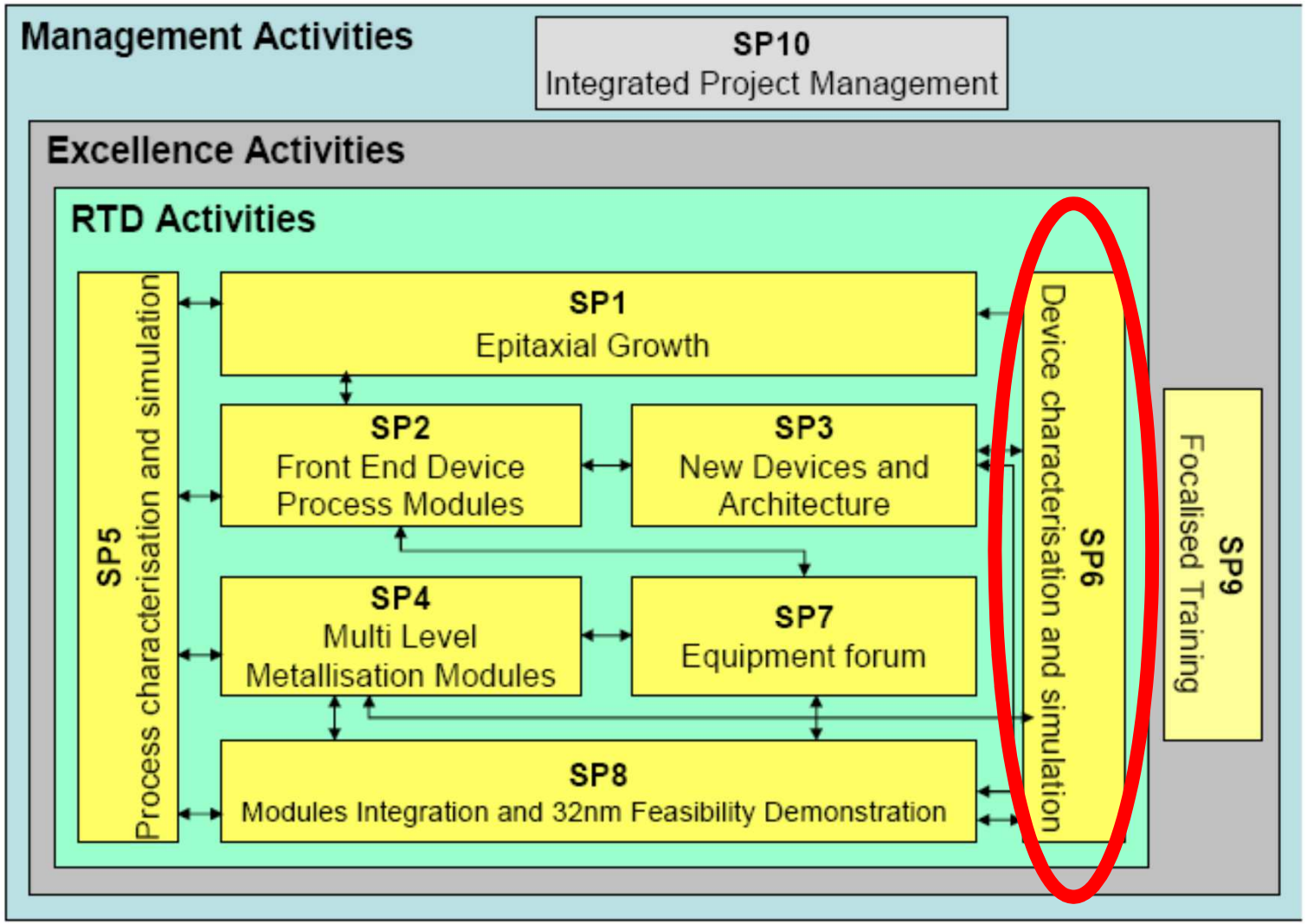


Alcuni passaggi importanti

- 2001: tentativo di aggregare i partner accademici europei per competere sugli ultimi 20Meuro di FP5.
- Enorme scetticismo verso accademia
- Player industriali rispondono con il progetto NESTOR
- Quale ruolo per i partner accademici ? Quale modello per le relazioni Industria-Accademia nel settore semiconduttori ?
- SINANO e NANOCMOS

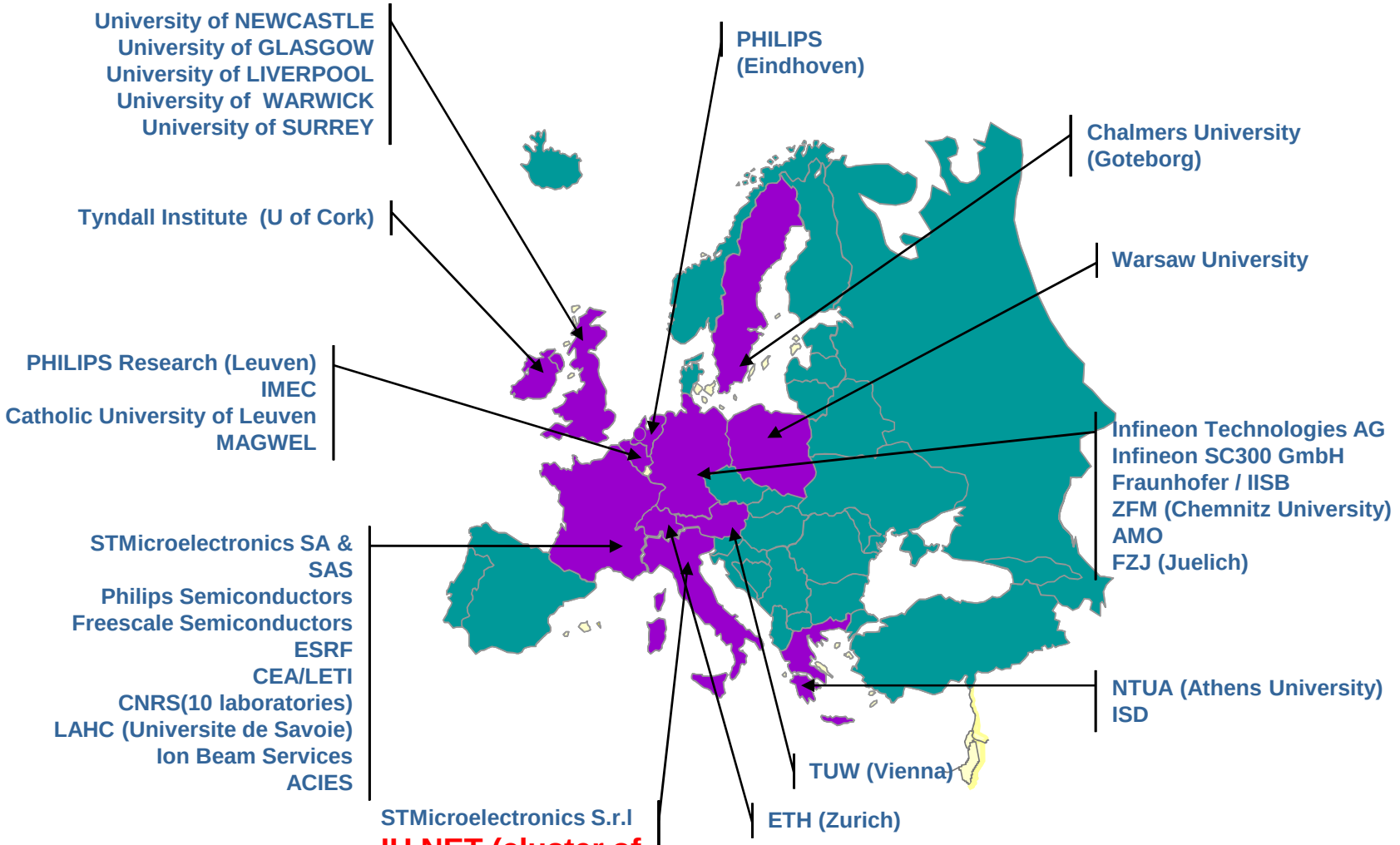
- Necessità di superare la frammentazione
- Necessità di superare il dualismo Industria-Accademia
- Cluster accademico «immerso» nel progetto

PULLNANO Organization



The PULLNANO Consortium

35 PARTERS in 12 EUROPEAN Countries



SP6 expected breakthroughs

- Advanced modeling and simulations

  - new physical models for transport and fluctuations

- TCAD simulation:

  - device design and specification, strain, benchmarking

- Compact modeling:

  - new compact models, transfer to MASTAR

- Electrical characterization:

  - mobility in short devices, high-k diel quality assessment

SP6 - WP4 Objectives

- Develop advanced physical models addressing the needs foreseen for the 32 nm and 22nm TN:
  - strained silicon / thin semiconductor films
  - adoption of different crystal orientations for the channel
  - high-k gate dielectrics
  - Sources of fluctuations (dopants, traps, dielectric and silicon layer thickness, line-edge roughness, …)
- Implement the models in device simulators
- Compare different device architectures and technological options
- Compare the simulation tools

PULLNANO at a glance

Total funding by EC: 25 M€ for 30 months

Cluster 6.4 (first 18 months):

- IU.NET 0.55
- ETH 0.16
- UGLA 0.15
- WUT 0.07
- CNRS 0.07

IU.NET (first 18 months) : 120 p.months

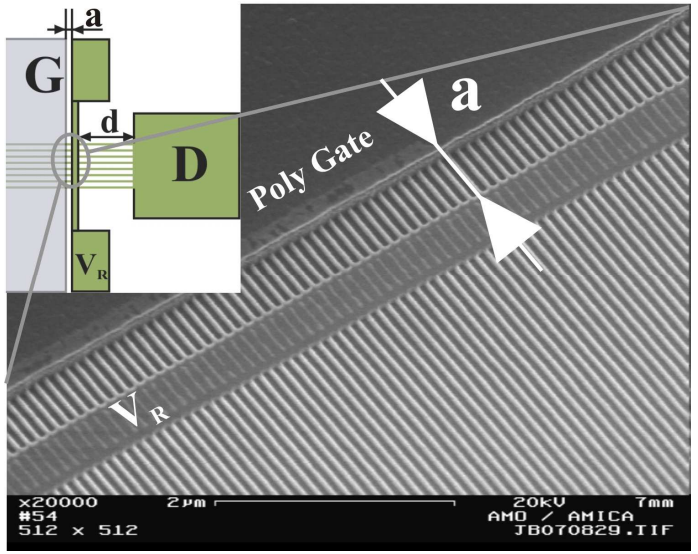
IU.NET internal breakdown

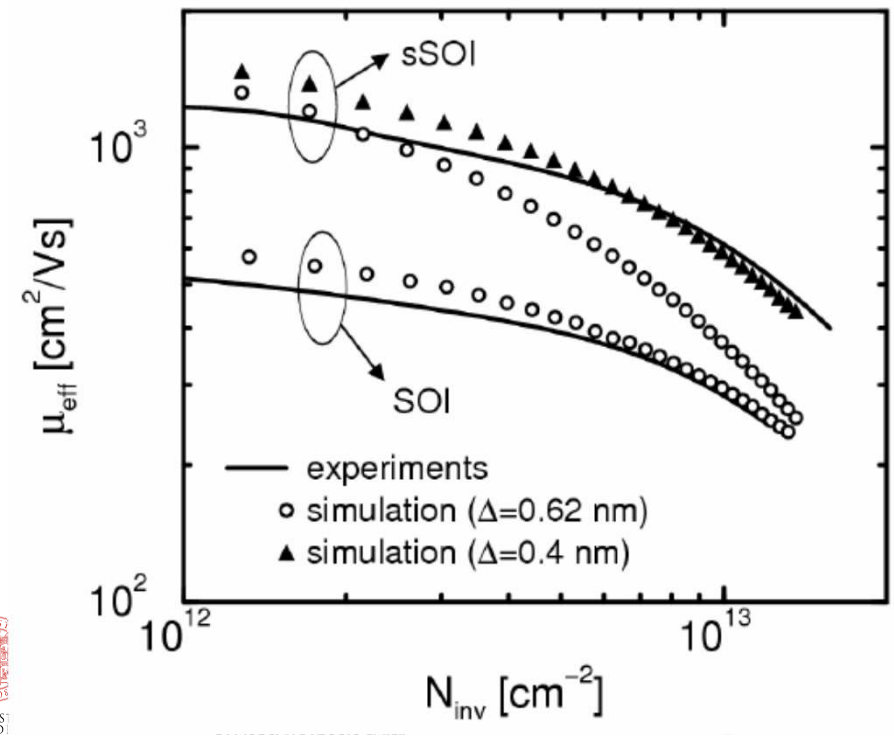
- University of Bologna ≈ 0.32
- University of Udine ≈ 0.32
- Politecnico of Milan ≈ 0.16
- University of Pisa ≈ 0.16
- IU.NET ≈ 0.04

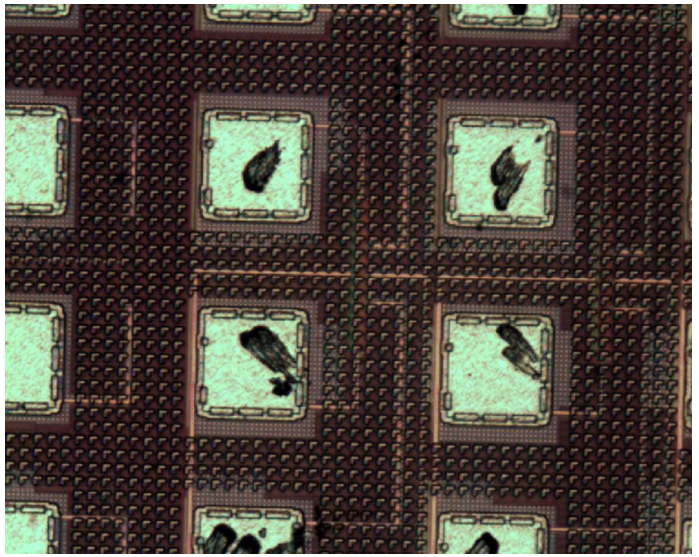
Test Structures

Mobility test structures in planar and FinFET technology (different substrates, strain levels, crystal orientation, etc…)

Porting of the test structures into STM, LETI and IMEC mask sets







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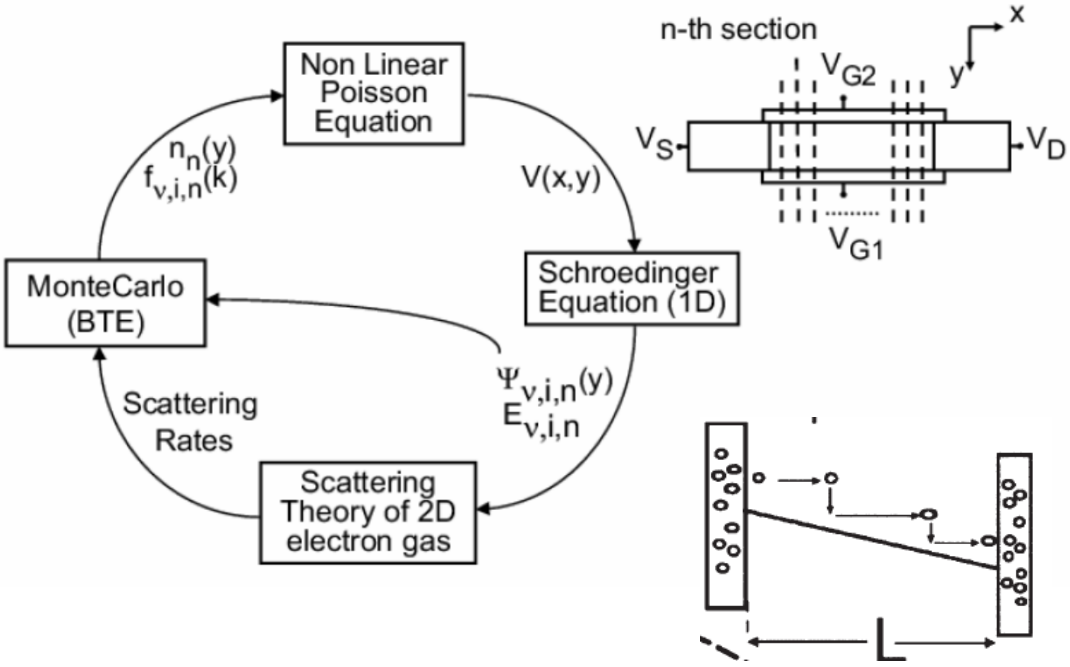
MSMC: development and applications (UD)

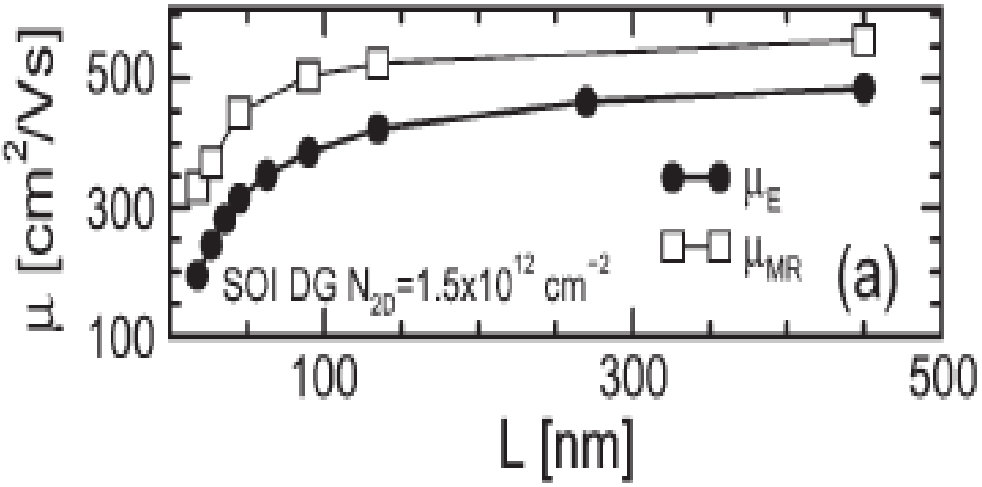
Develop transport models to predict the I_{ON} of nanoscale devices
- ballistic mobility
- high-k dielectrics
- strain engineering

Understand the effectiveness of the technology boosters and the distance from the theoretical limits

Benchmarking characterization techniques

Comparison between 3DMC and MSMC models



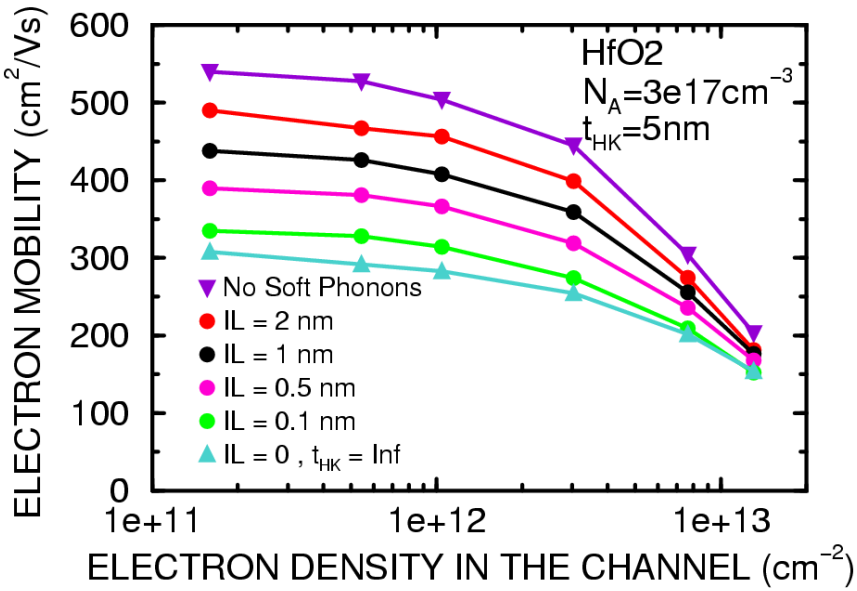


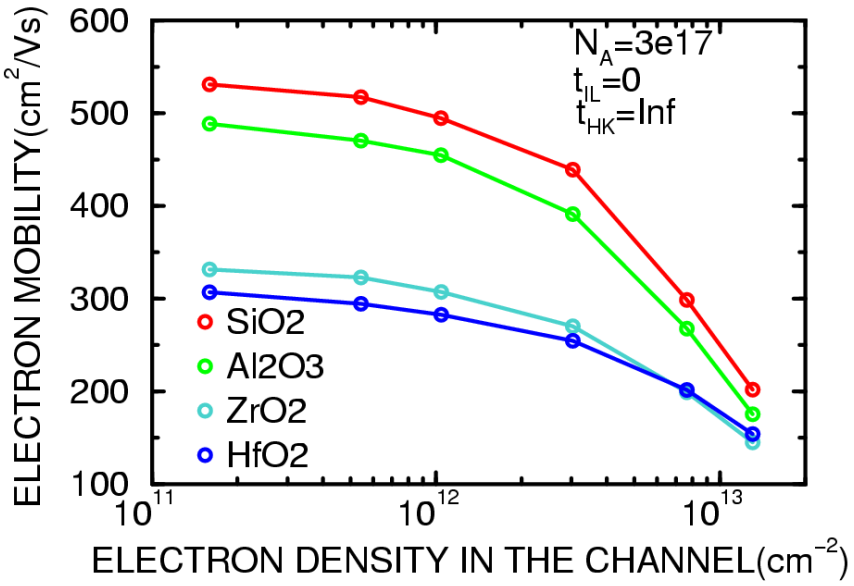
MSMC Physical Models (UD)

Introduction of High-k materials in the gate stack

Develop new physical models and evaluate the impact of different technology options on the channel mobility.

Remote optical phonon scattering





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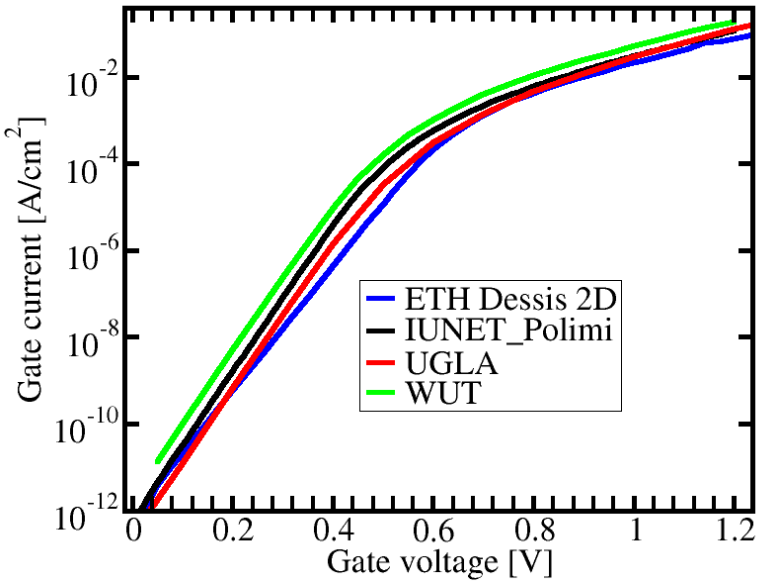
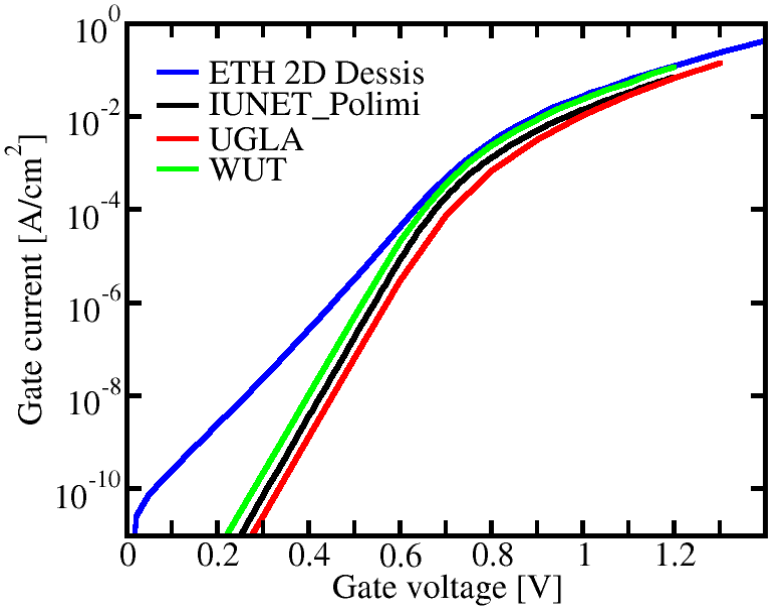
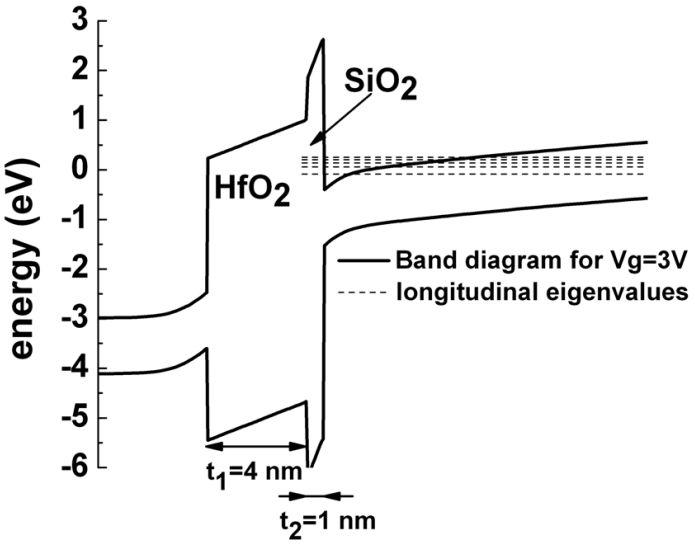
Comparison of gate currents in high-K stacks (POLIMI)

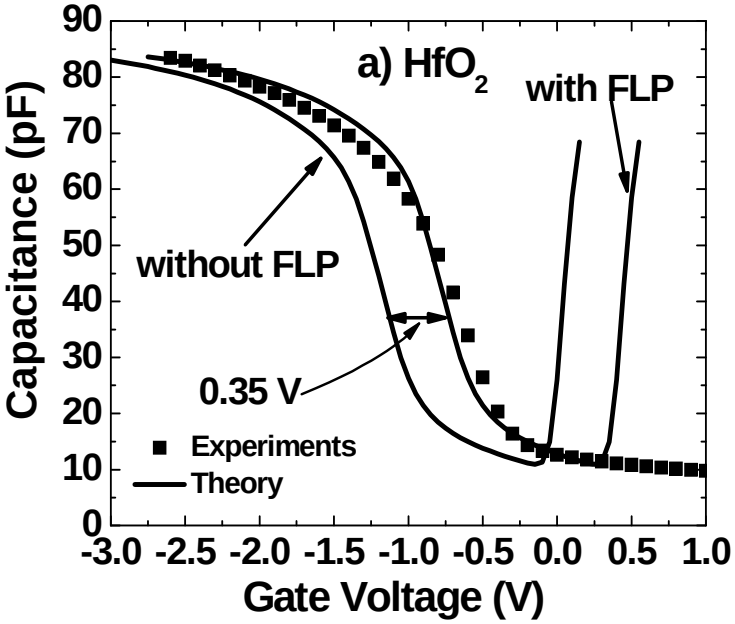


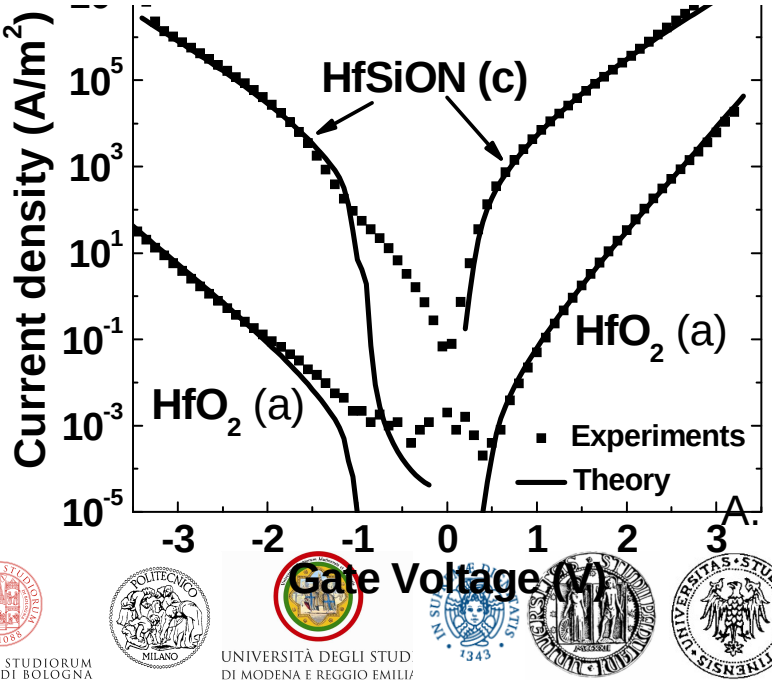


- Extension of the work performed in SINANO (tunneling contribution only)
- Results reported in D6452

Transport in high-k stacks (PISA)







Par. extracted for HfO_2 , HfSiON and SiON			
	HfO2	*HfSiON*	*SiON*
Electron affinity	1.575 eV	1.97 eV	1.27 eV
Electron eff mass	$0.08m_0$	$0.24m_0$	$0.45\ m_0$
ε_r	25	11	5
FLP	0.35 V	0.13 V	-

A. Campera, F. Crupi, G. Iannaccone, TED 54, 83 2007

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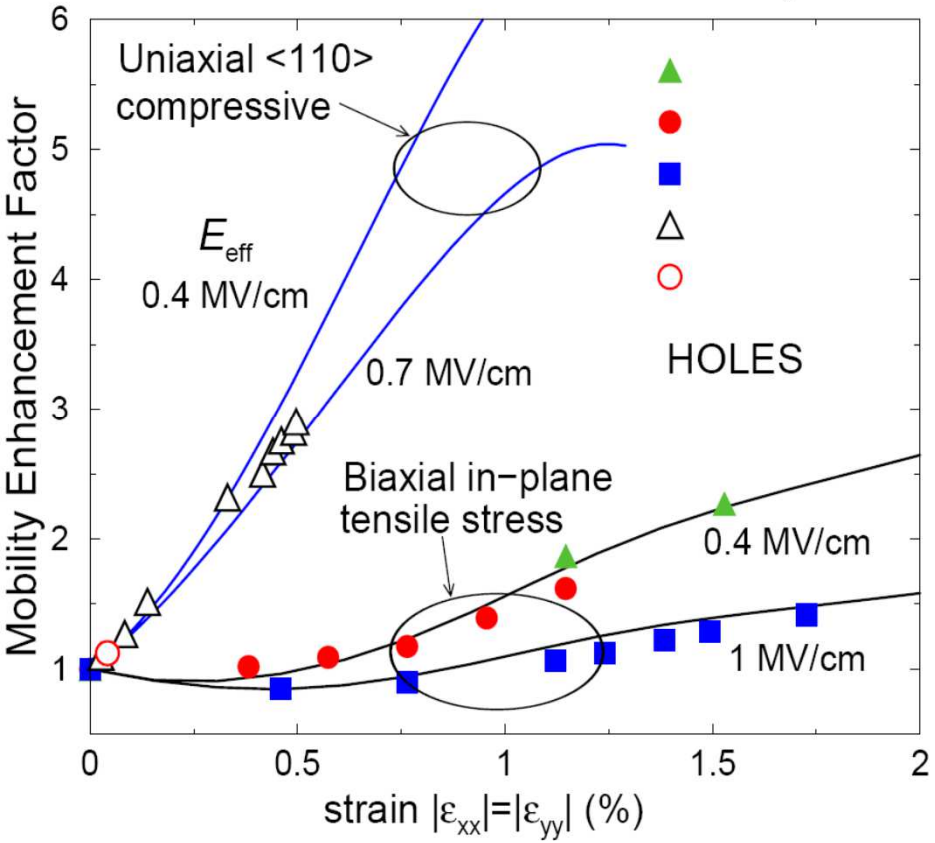
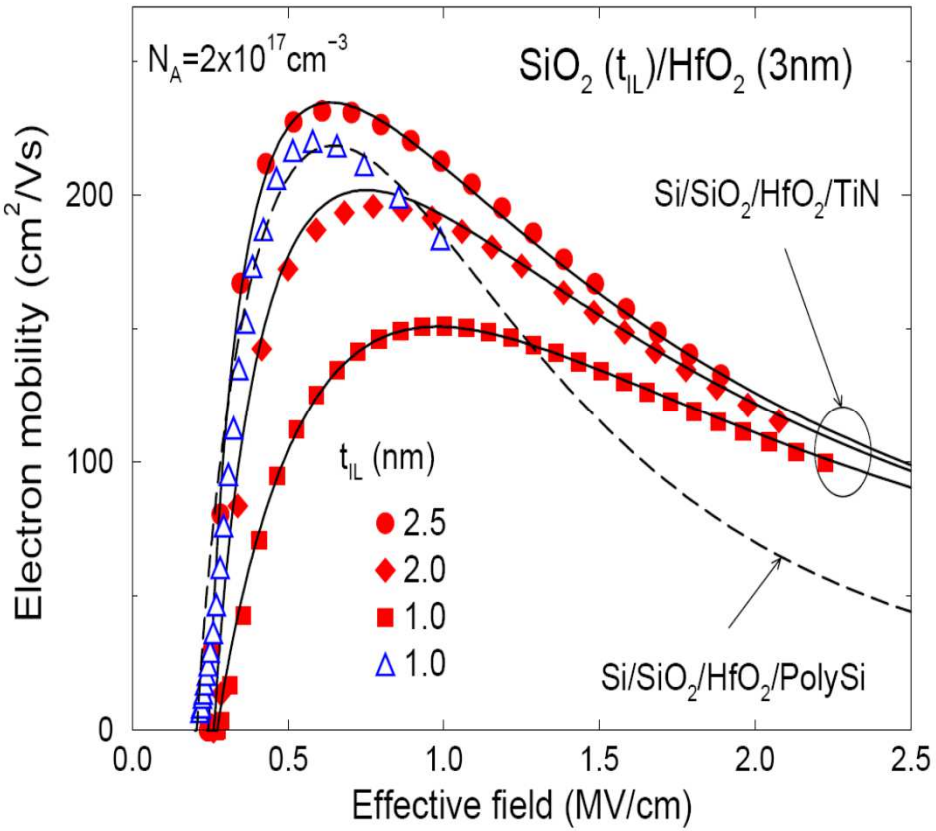
Analytical Mobility Models (BO)

- Analytical mobility models for PDE based simulators
- Calibration w.r.t. extensive sets of experiments

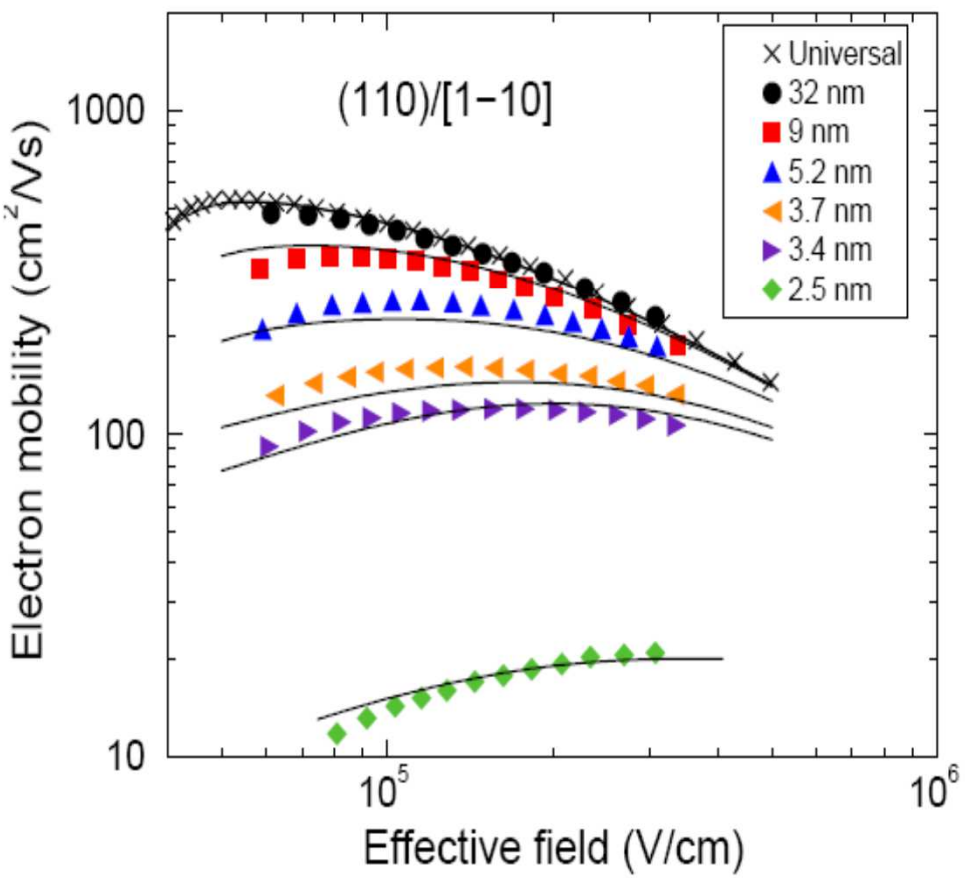
Electron and hole mobility for strained silicon and high-k stacks

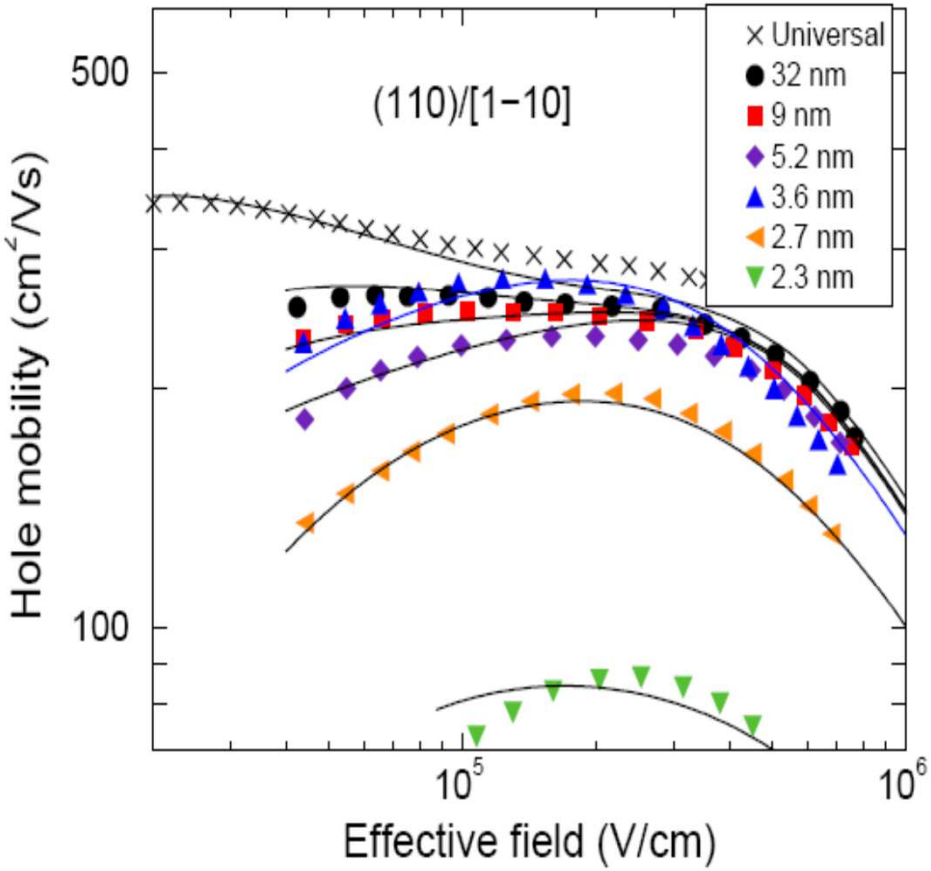




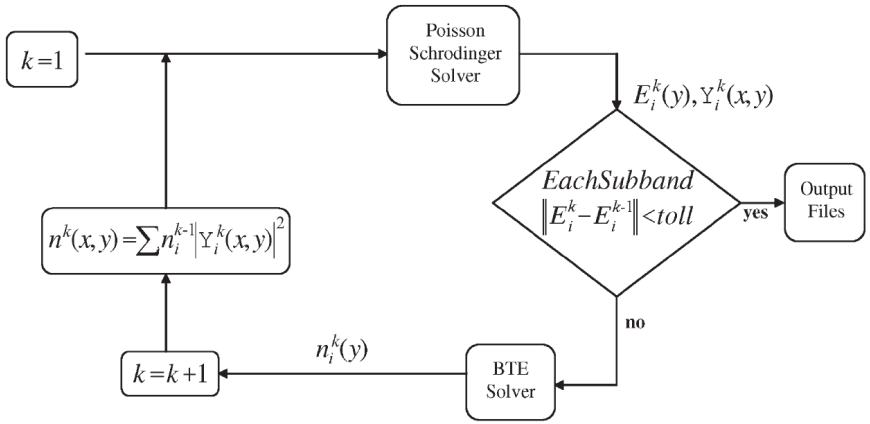
Analytical Mobility Models (BO)

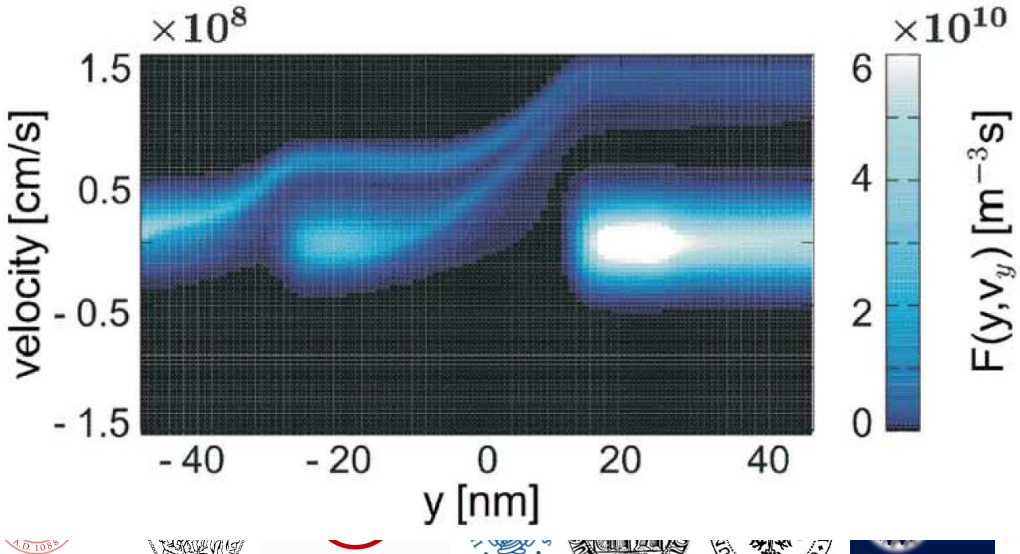
Electron and hole mobility for ultra-thin body and different substrate/channel orientations





Direct solution of the BTE for nanoMOSFETs (PISA)





- Reduced size of the phase space
- Deterministic solution of the BTE per subband
- Preliminary results based on two simplyfing assumptions:
  - No intersubband mixing
  - relaxation time approximation
- S. Scaldaferri et al., IEEE-TED, vol. 54, 2901 (2007).

Model benchmarking

Solid-State Electronics 53 (2009) 1293–1302

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

A comparison of advanced transport models for the computation of the drain current in nanoscale nMOSFETs

P. Palestri [a,*], C. Alexander [b], A. Asenov [b], V. Aubry-Fortuna [d], G. Baccarani [c], A. Bournel [d], M. Braccioli [e], B. Cheng [b], P. Dollfus [d], A. Esposito [f], D. Esseni [a], C. Fenouillet-Beranger [j,k], C. Fiegna [e], G. Fiori [h], A. Ghetti [g], G. Iannaccone [h], A. Martinez [b], B. Majkusiak [i], S. Monfray [j], V. Peikert [f], S. Reggiani [c], C. Riddet [b], J. Saint-Martin [d], E. Sangiorgi [e], A. Schenk [f], L. Selmi [a], L. Silvestri [c], P. Toniutti [a], J. Walczak [i]

Acknowledgment

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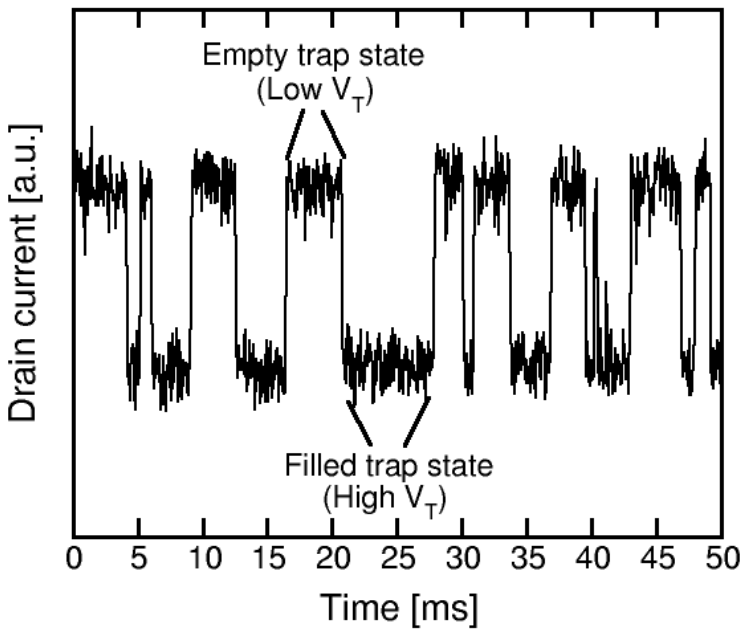
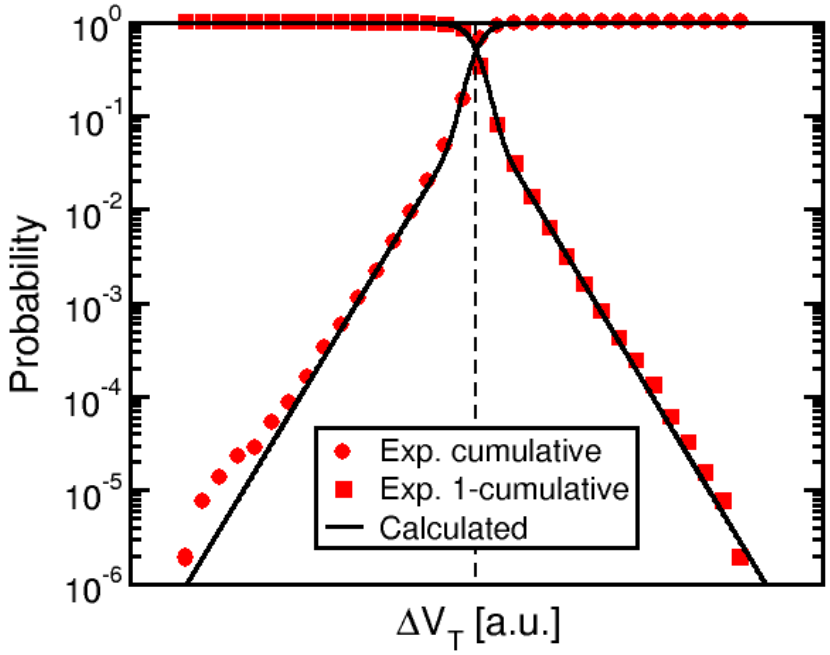
[j] ST Microelectronics, Crolles, France
[k] CEA/MINATEC/LETI, 17 rue des Martyrs, 38054 Grenoble, France

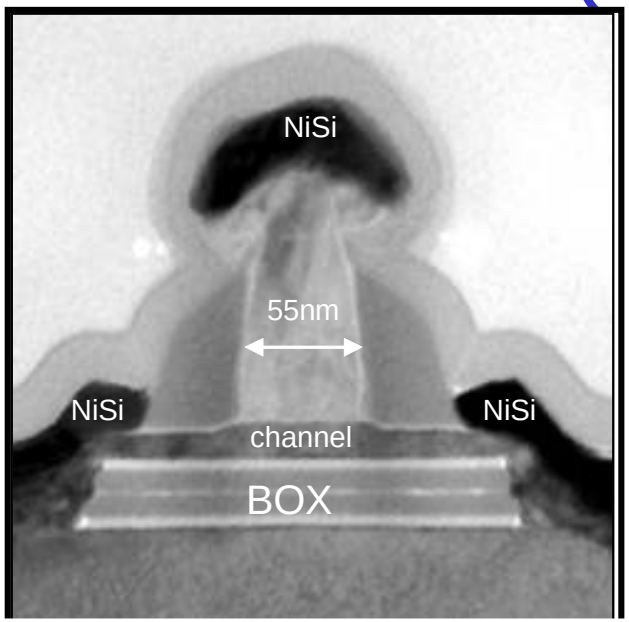
Fluctuations at device level (POLIMI)

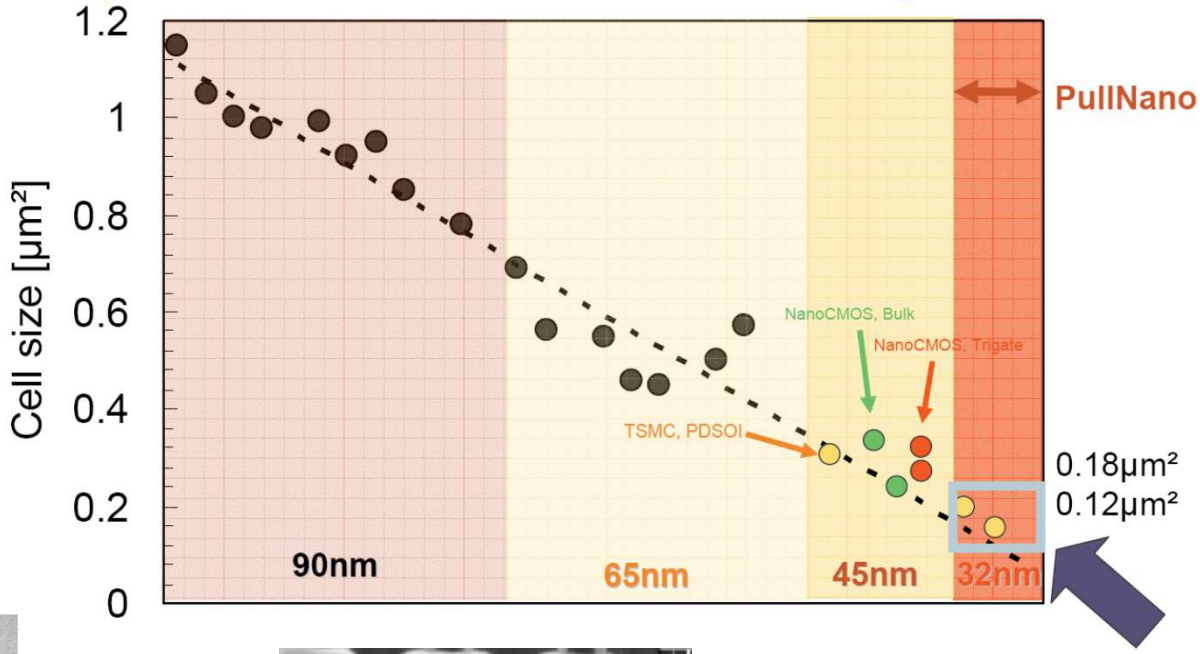


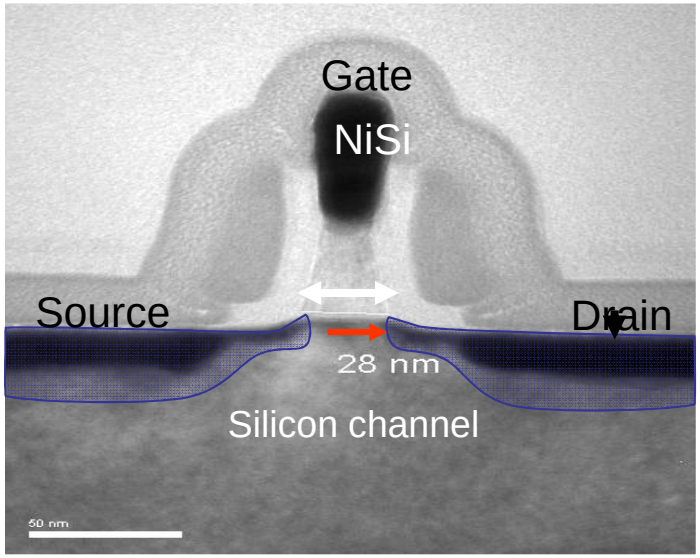


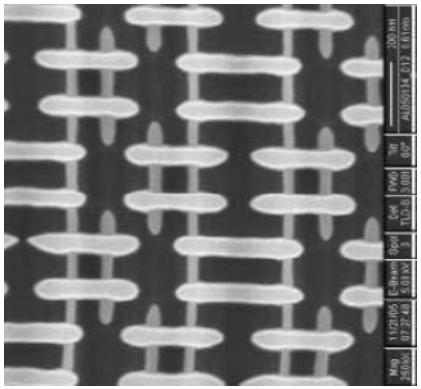
- Analysis of RTN in Flash NOR devices
- Results reported in D6411

Achievements
(in spite of NXP default)









The End

IU.NET e PULLNANO (+/-)

- Sostanziale aderenza al piano delle attività
- Difficoltà nel giustificare alcune attività (pertinenza, overlap)
- Positiva evoluzione di alcune attività durante il progetto
- Definire con chiarezza ad inizio progetto chi fa cosa
- Convergenza dei temi di ricerca tra gruppi di IUNET
- Creazione di opportunità per nuovi partner IUNET

- Un nuovo modello di relazioni Industria-Accademia nei progetti
- Coagulazione di un gruppo di partner accademici «accreditati»