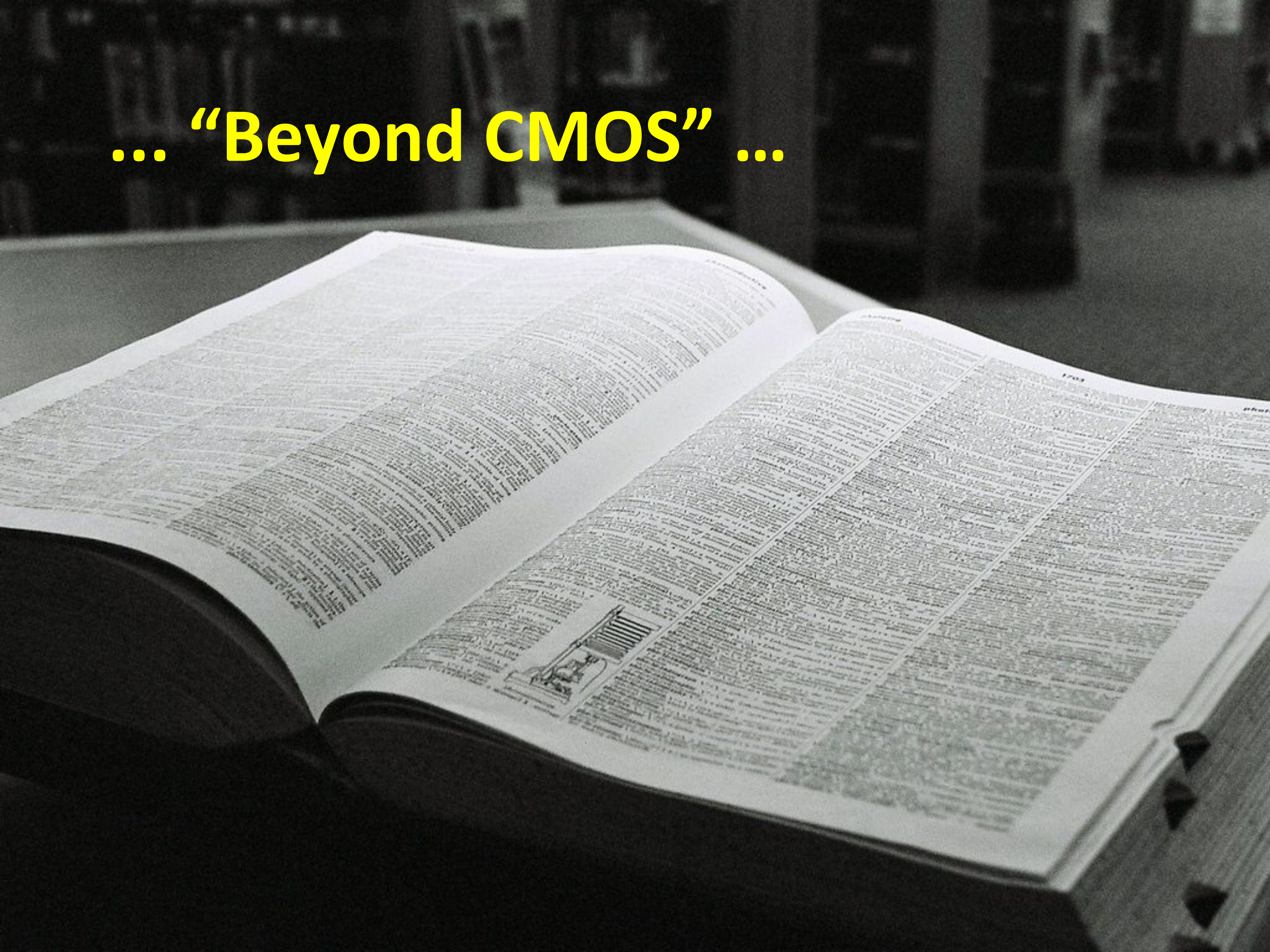
Beyond CMOS

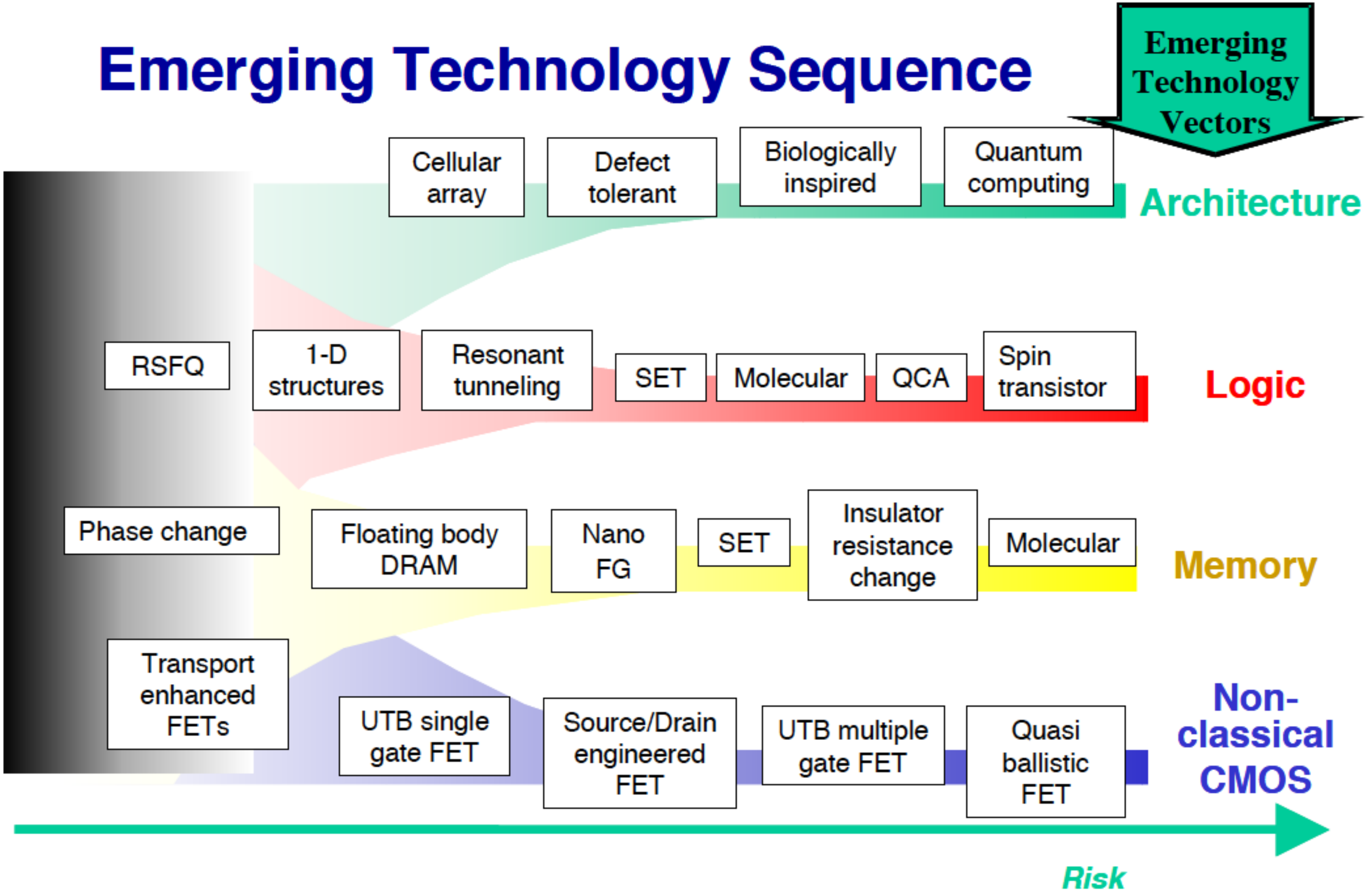
IU.NET in search of the next switch

Giuseppe Iannaccone, U. Pisa

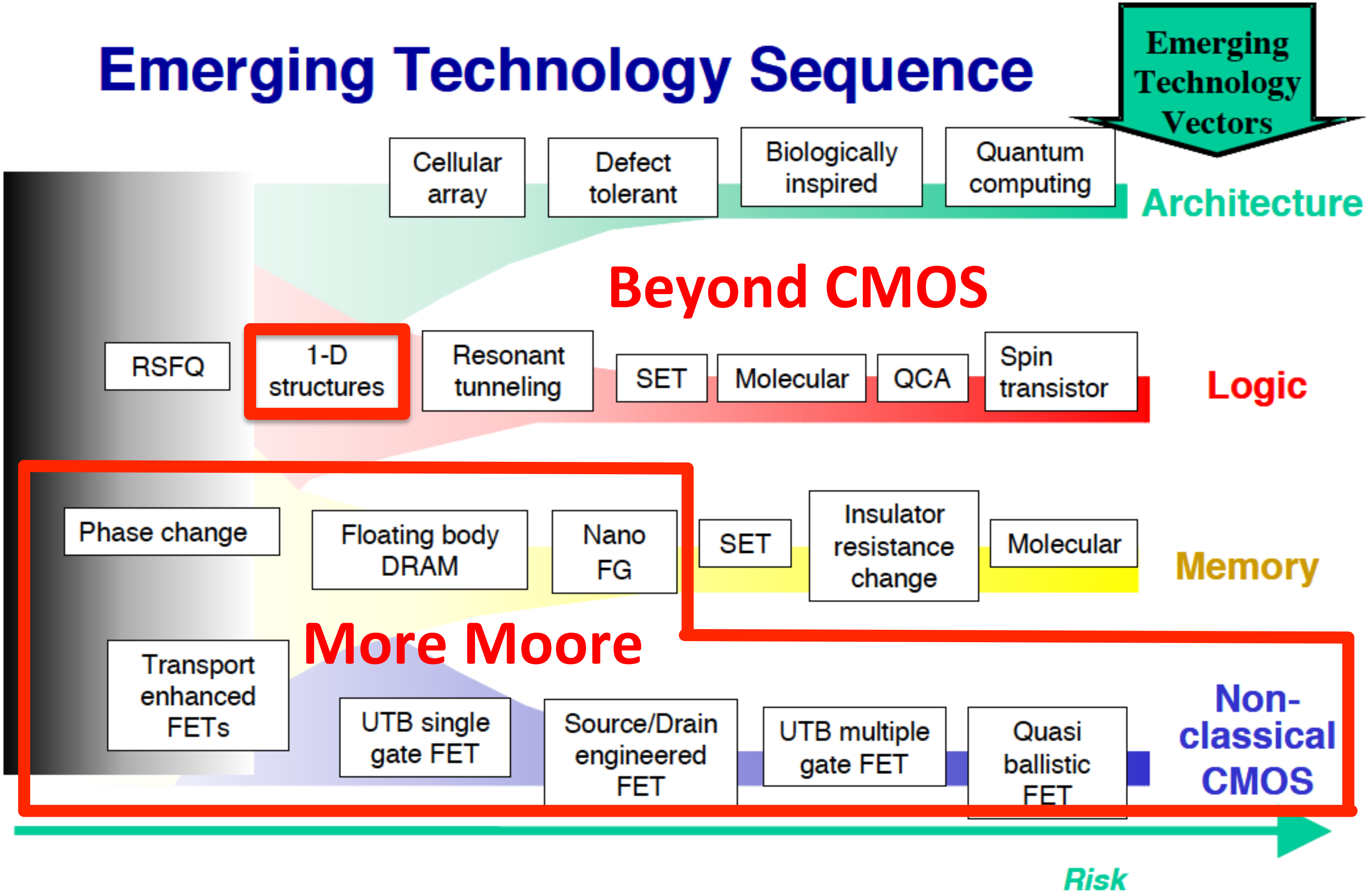
… “Beyond CMOS” …



From ITRS **2003**



From ITRS **2003** (→ 22 nm)



Emerging Technology Sequence

Emerging Technology Vectors

Cellular array

Defect tolerant

Biologically inspired

Quantum computing

Architecture

Beyond CMOS

RSFQ

1-D structures

Resonant tunneling

SET

Molecular

QCA

Spin transistor

Logic

Phase change

Floating body DRAM

Nano FG

SET

Insulator resistance change

Molecular

Memory

More Moore

Transport enhanced FETs

UTB single gate FET

Source/Drain engineered FET

UTB multiple gate FET

Quasi ballistic FET

Non-classical CMOS

Risk

First Call of FP7 (dec 2006)

After ENIAC SRA 2005

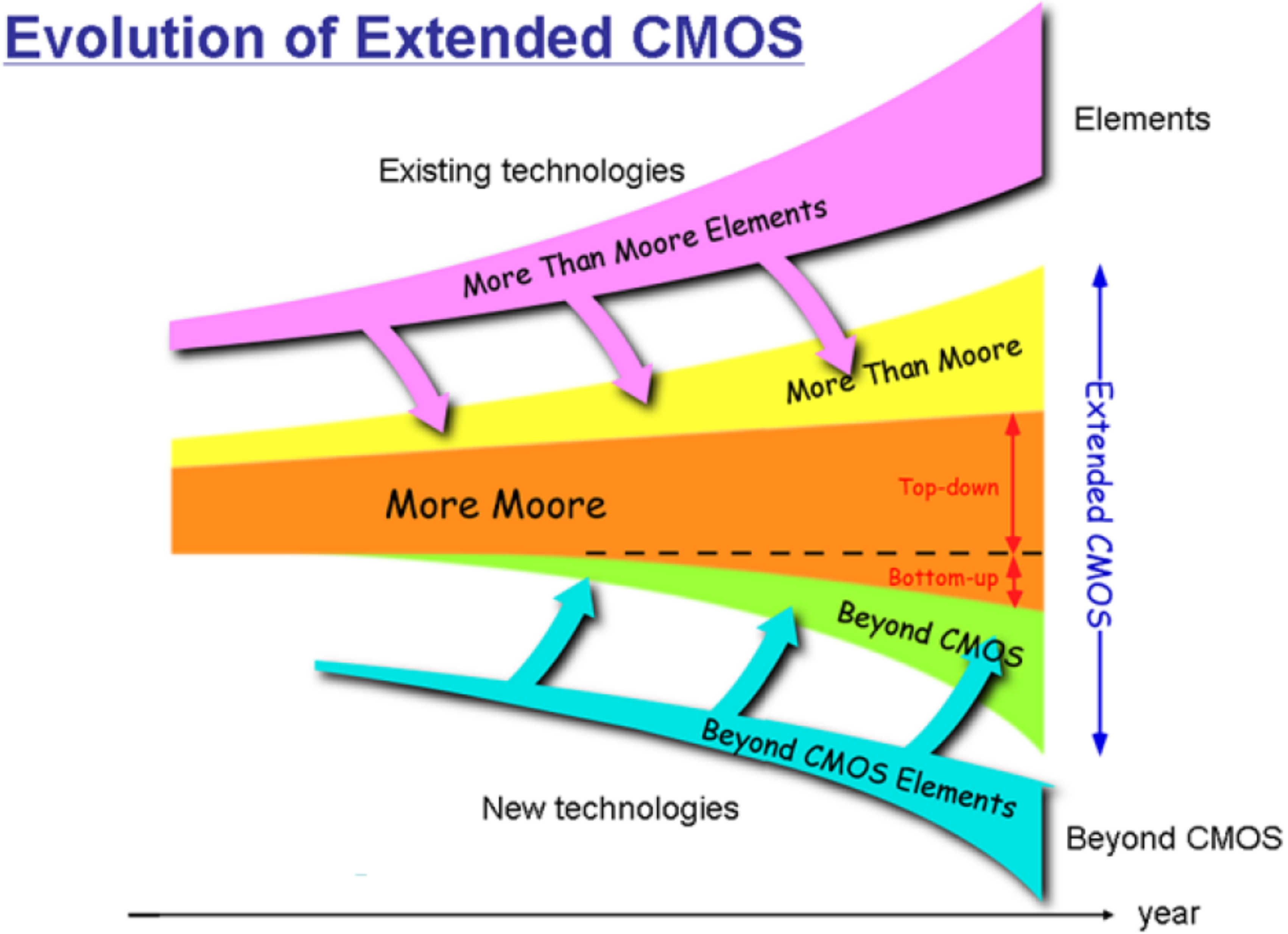
- “**More Moore**”:

  beyond 32 nm, digital SoCs
- “**More than Moore**”:

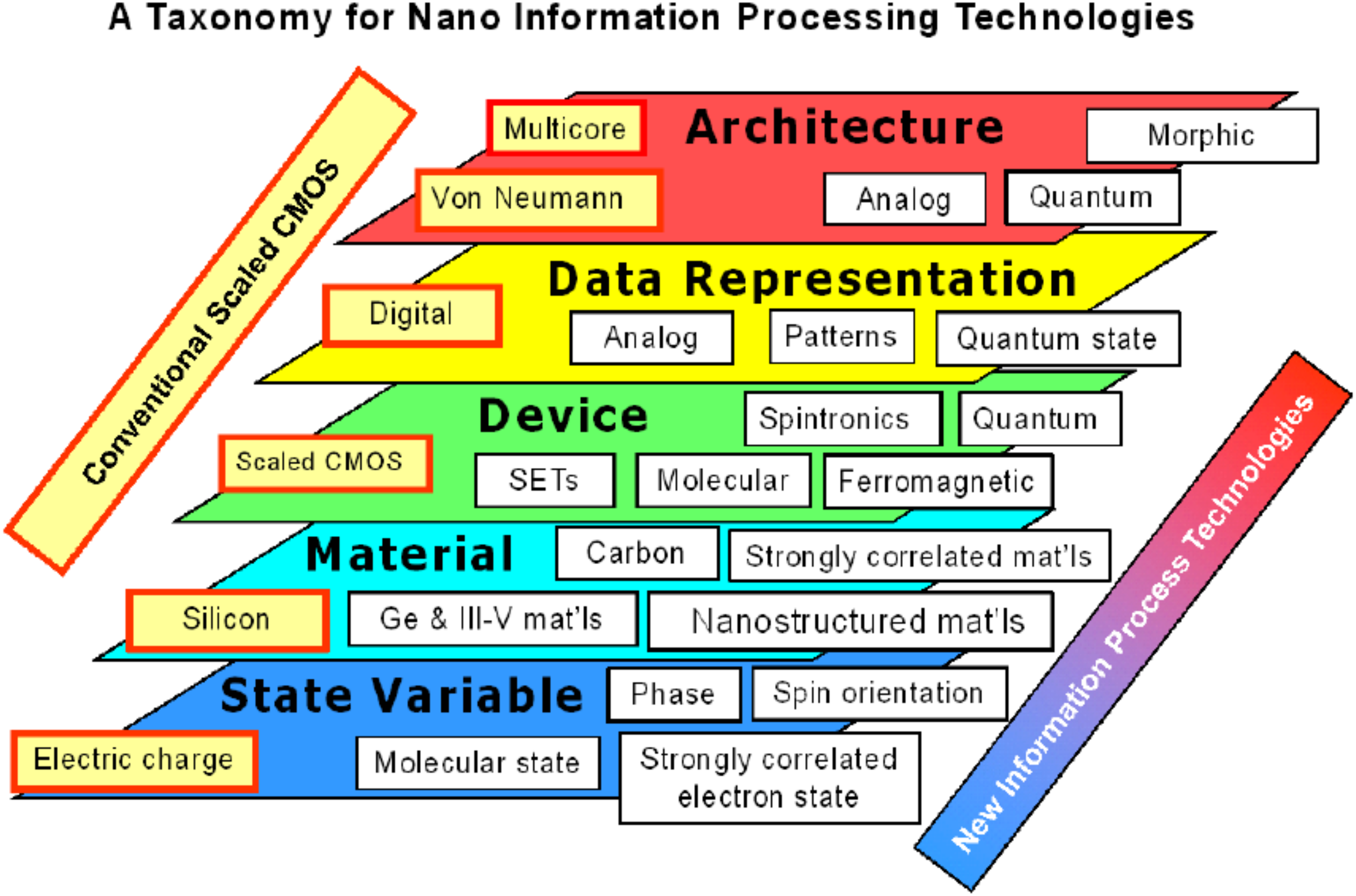
  heterogeneous SoPs
- “**Beyond CMOS**”:

  non-FET-based logic and memory (and their integration with CMOS).

From ITRS **2013**

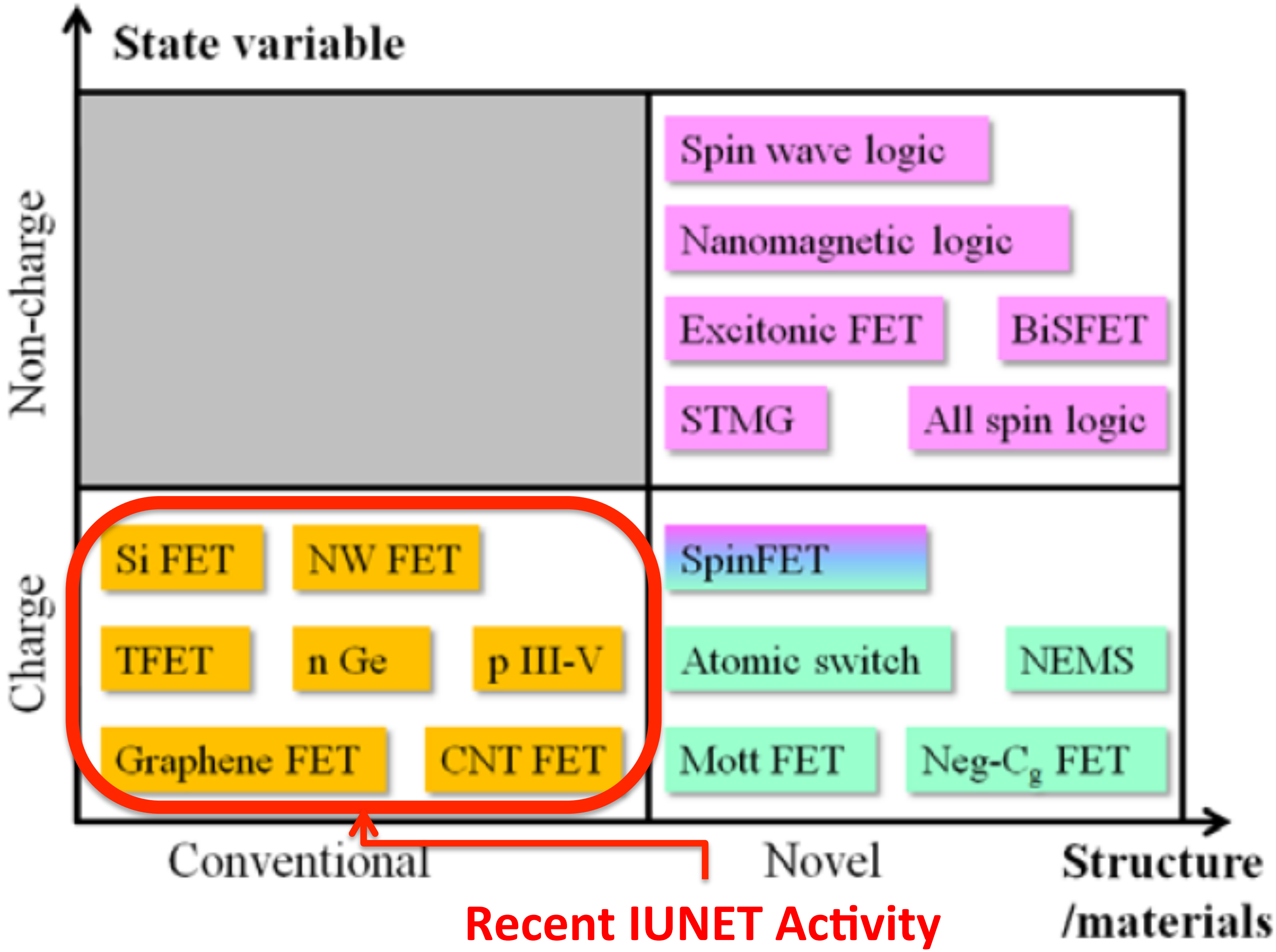


From ITRS 2013



From ITRS 2013

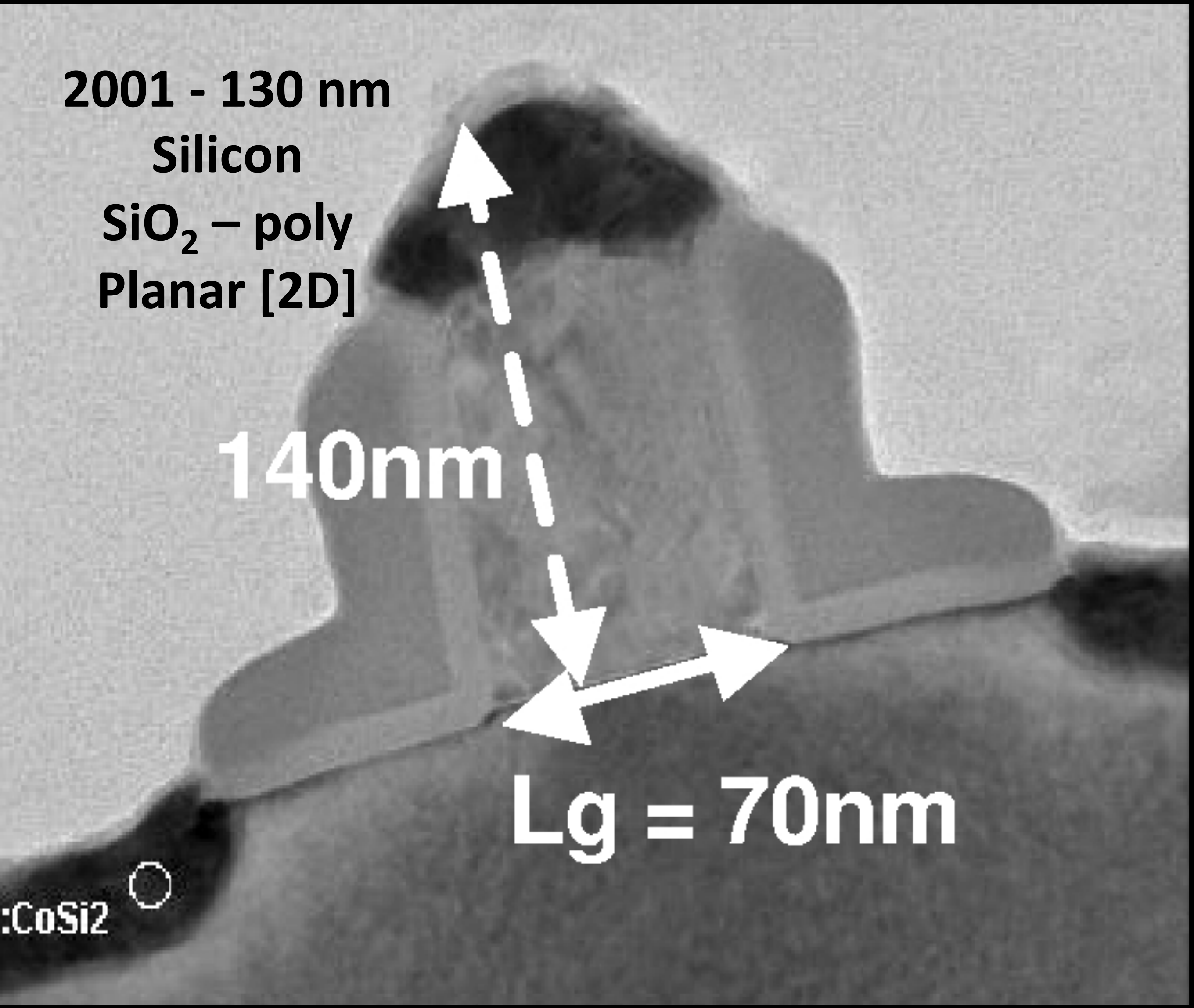
Taxonomy of options for emerging logic devices



Recent IUNET Activity

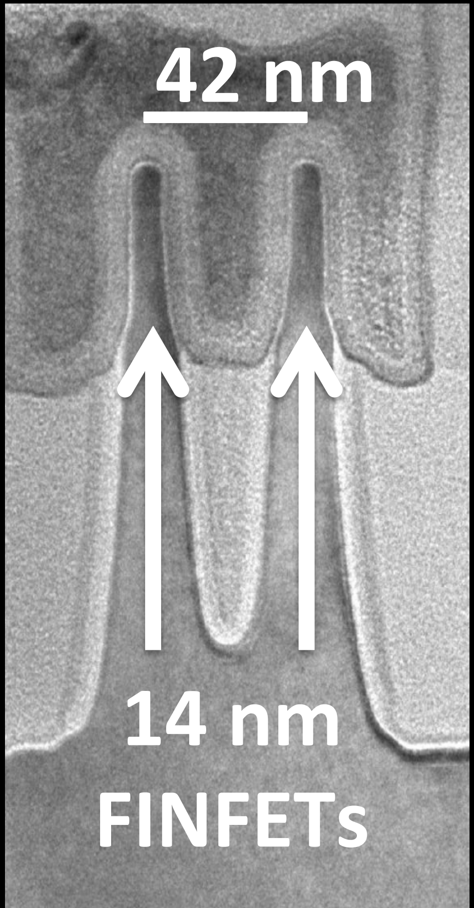
…We have nothing Beyond CMOS…

Are we already beyond CMOS?



2001 - 130 nm
Silicon
SiO_2 – poly
Planar [2D]

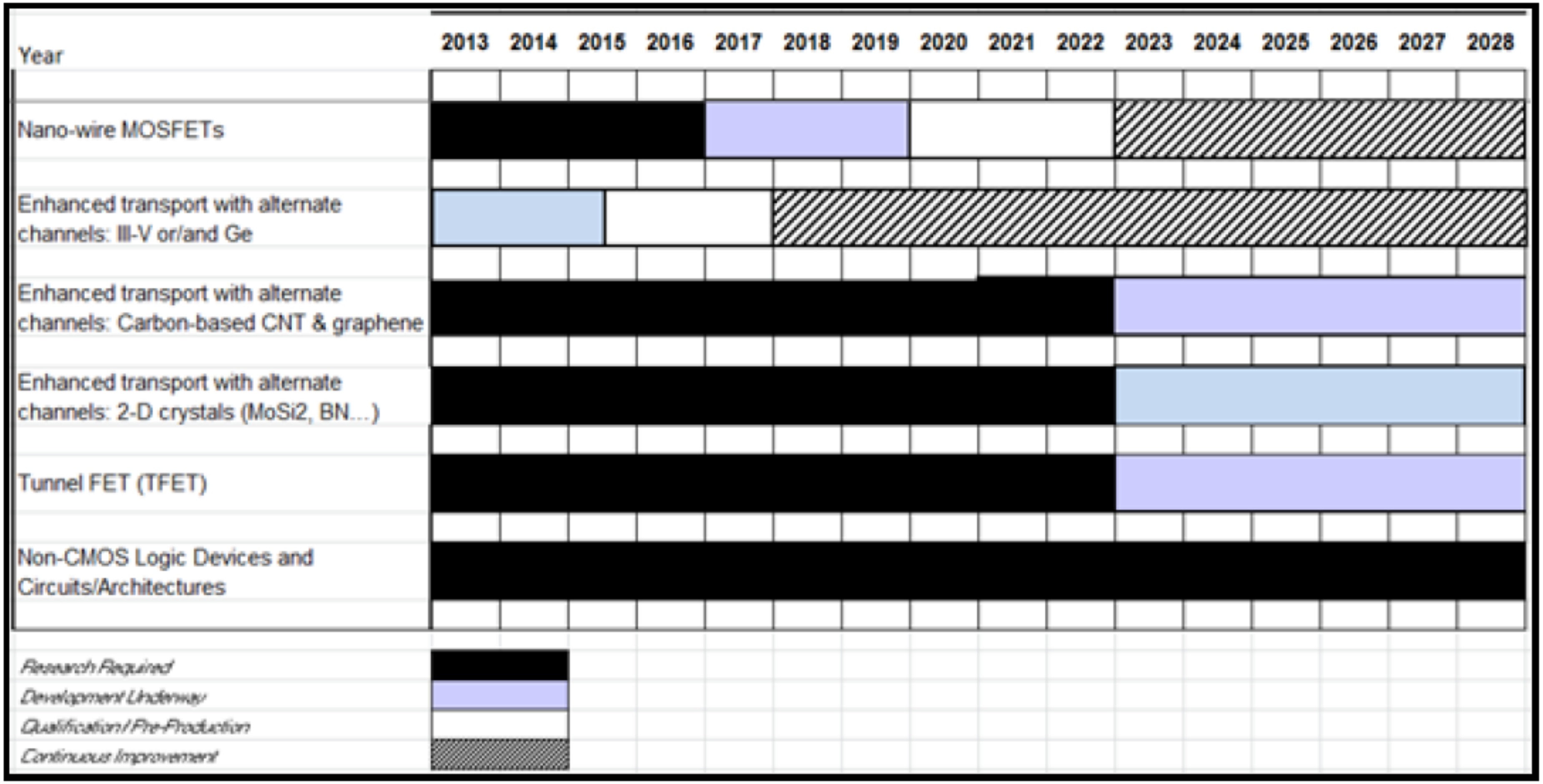
2014 -14 nm
Strained Si/Ge
HKMG - 3D



14 nm
FINFETs

From ITRS 2013 - PIDS chapter

[my note: PIDS = More Moore]



Year	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Nano-wire MOSFETs	■	■	■	■	🟪	🟪	🟪	□	□	□	▨	▨	▨	▨	▨	▨
Enhanced transport with alternate channels: III-V or/and Ge	🟦	🟦	🟦 □	□	□	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
Enhanced transport with alternate channels: Carbon-based CNT & graphene	■	■	■	■	■	■	■	■	■	■	🟪	🟪	🟪	🟪	🟪	🟪
Enhanced transport with alternate channels: 2-D crystals (MoSi2, BN...)	■	■	■	■	■	■	■	■	■	■	🟦	🟦	🟦	🟦	🟦	🟦
Tunnel FET (TFET)	■	■	■	■	■	■	■	■	■	■	🟪	🟪	🟪	🟪	🟪	🟪
Non-CMOS Logic Devices and Circuits/Architectures	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■

Research Required ■

Development Underway 🟪

Qualification/Pre-Production □

Continuous Improvement ▨

IUNET Projects with focus on ““““**Beyond CMOS**”””” (logic)

- Nanosil (FP6):
  - Nanowire Transistors, graphene, Tunnel FETs
- GRAND (FP7):
  - Graphene-based devices: GFETs and GNRFETs

Also 1 SpinFET example

- Steeper (FP7):
  - Tunnel FETs
- GRADE (FP7):
  - Graphene-based devices: GFETs and GBTs

Non FET

Pre-IUNET: Quadrant (FP4), Answers, NanoTCAD (FP5), Sinano (FP6)

QCA

QCA

SET
Single Molecule

SpinFET

Main role of IUNET in “Beyond CMOS” projects

Use modeling and simulation to

- *propose* ***new device concepts****,*
- ***Explore*** *technology options,*
- ***Benchmark*** *and optimize device and technology proposals*

Main role of IUNET in "Beyond CMOS"

True multisciplinarity required:
Engineering + Physics + Chemistry

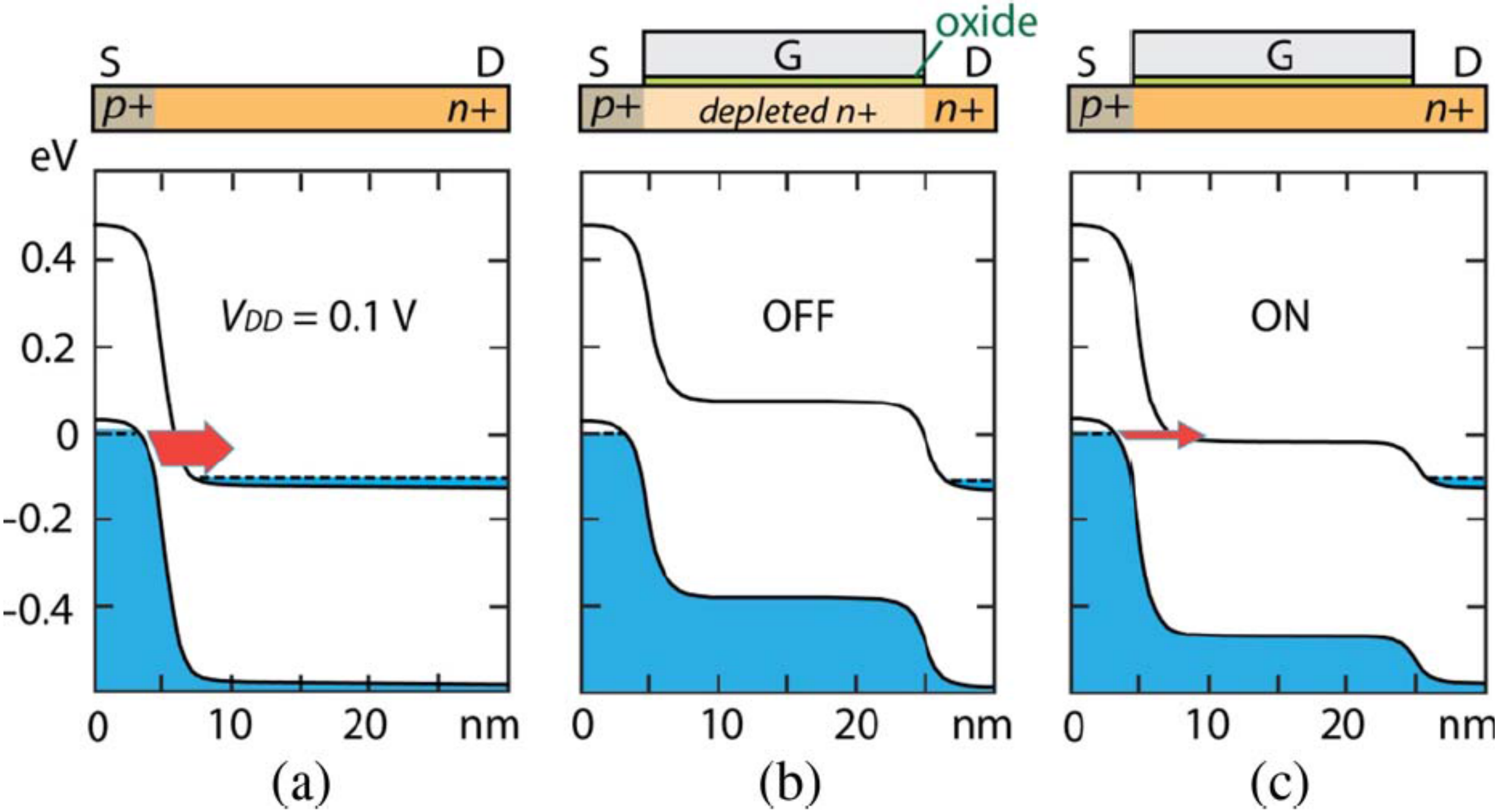
Use modeling and simulation to

- *propose* ***new device concepts****,*
- ***Explore*** *technology options,*
- ***Benchmark*** *and optimize device and technology proposal*

We should try to be competitive also in characterization and fabrication

TFET principle of operation

S. Banerjee et al. EDL 1987 (TI)
W. Hansch, several papers in 2000-2003 (TUM)



Credit: Figure from A. C. Seabaugh, Q. Zhang, Proc. IEEE 98, 2095 (2010)

Tunnel FET

- Main promise: **low V_{DD} operation → Low DPI**
- Small gap is an advantange → higher I_{ON}

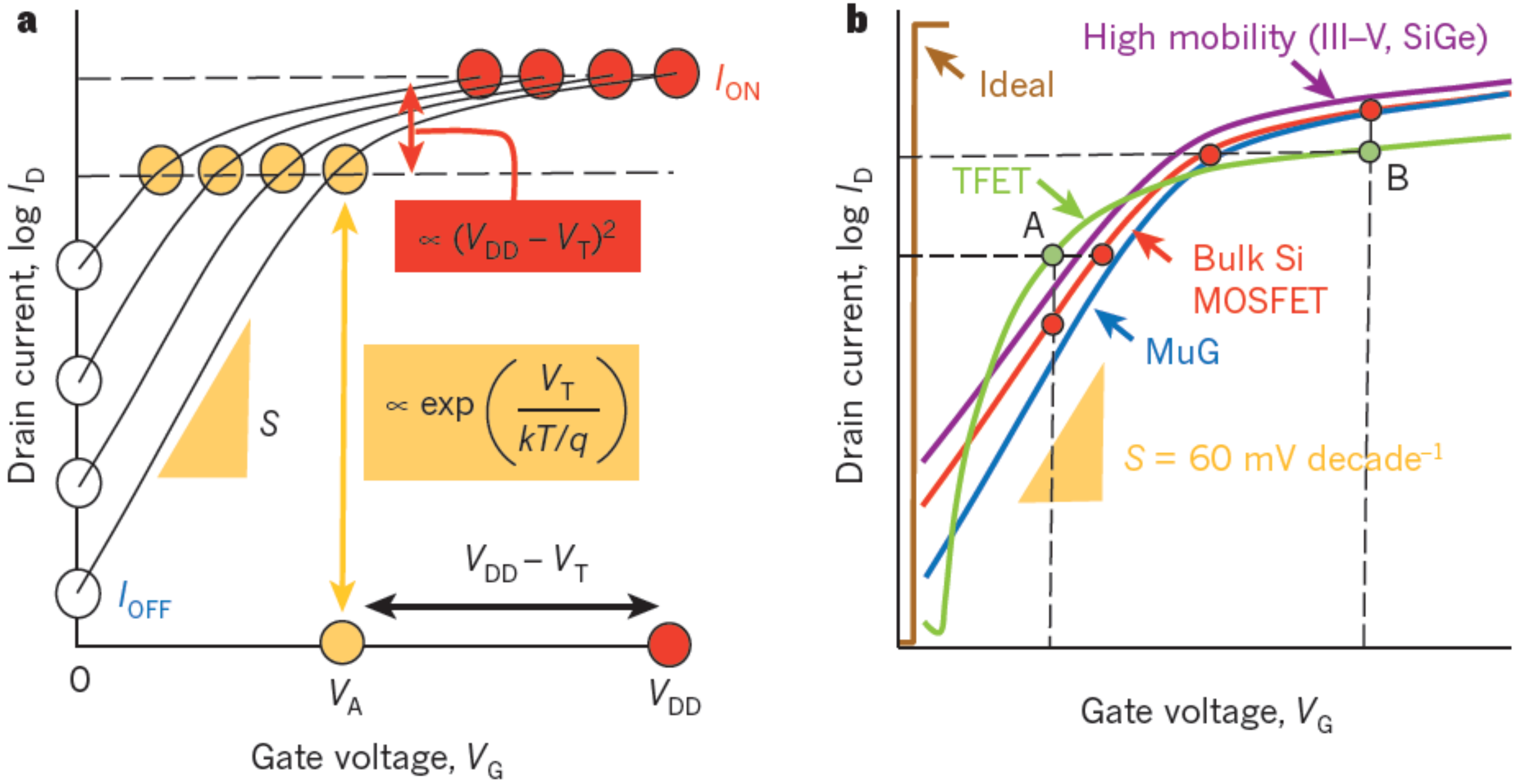
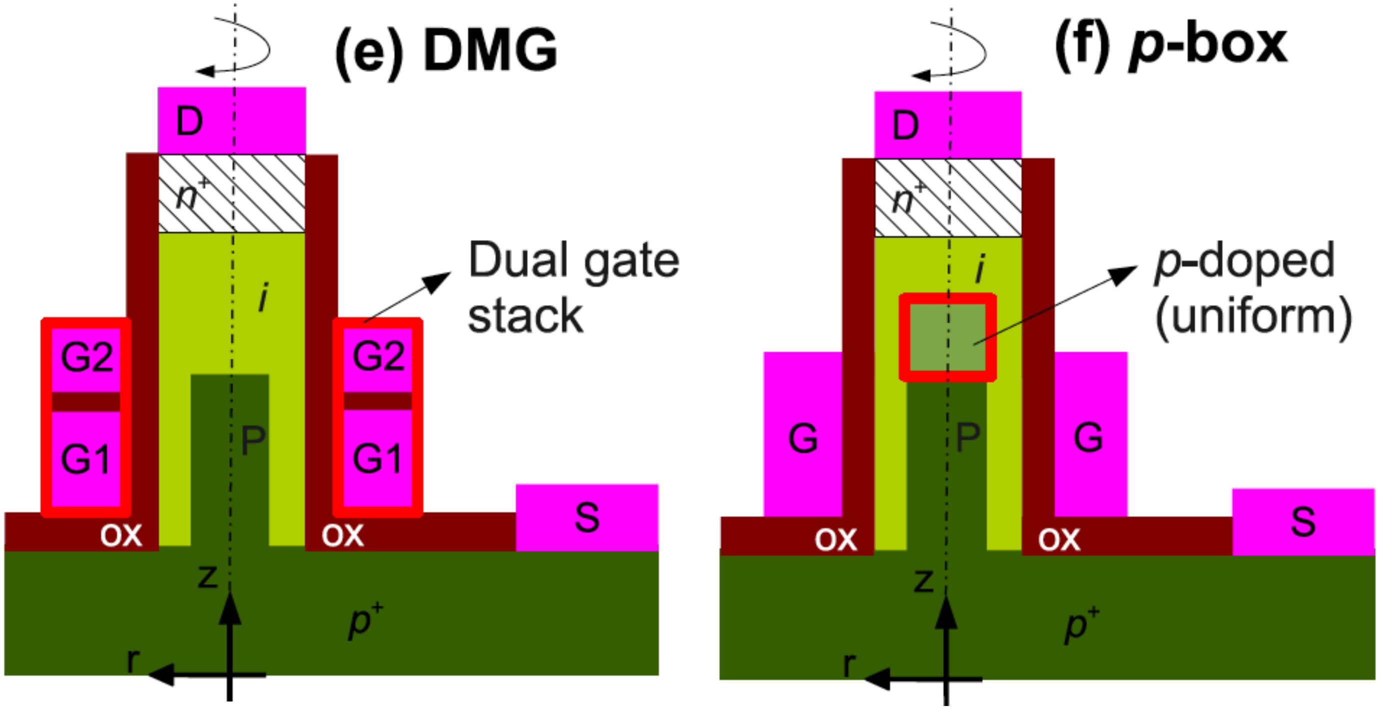


Figure Credits: Ionescu et al. Nature 479, 329 (2011)

InAs TFET optimization to meet ITRS 2020

Beneventi et al. IEEE TED 61, 778 (2014) - BOLOGNA

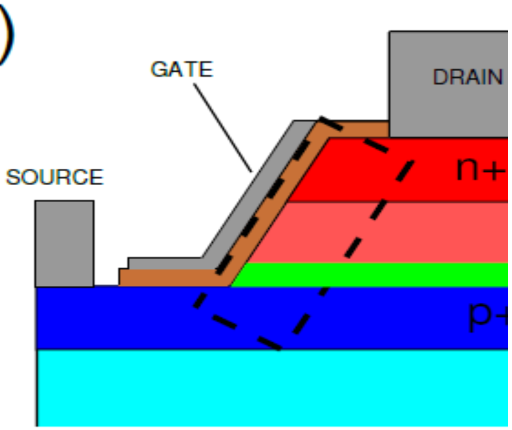


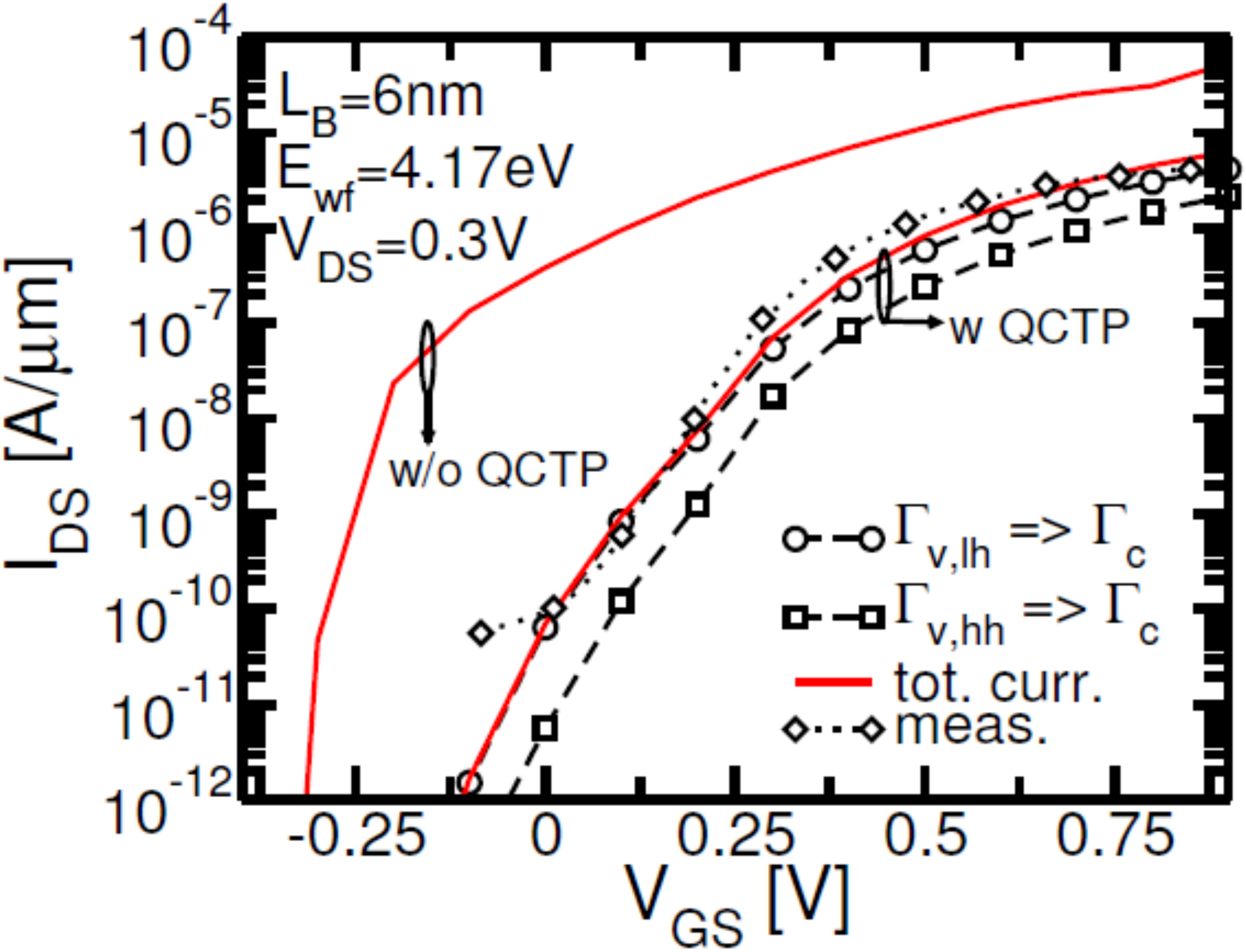
	ITRS 2020			OPT-DMG		
spec	LSTP	LOP	HP	LSTP	LOP	HP
V_{DD} [V]	0.67	0.53	0.68	0.5	0.5	0.5
I_{OFF} [nA/μm]	0.01	5	100	0.01	5	100
I_{ON} [mA/μm]	0.600	0.784	1.916	1.322	1.650	1.985
I_{ON}/I_{OFF}	6.0×10^7	1.5×10^5	1.9×10^4	1.3×10^8	3.3×10^5	2×10^4
τ (multi-gate) [ps]	0.58	0.35	0.19	0.94	0.68	0.31

Heterojunction III-V TFET

Modeling: UDINE con MC + BTBT (WKB)

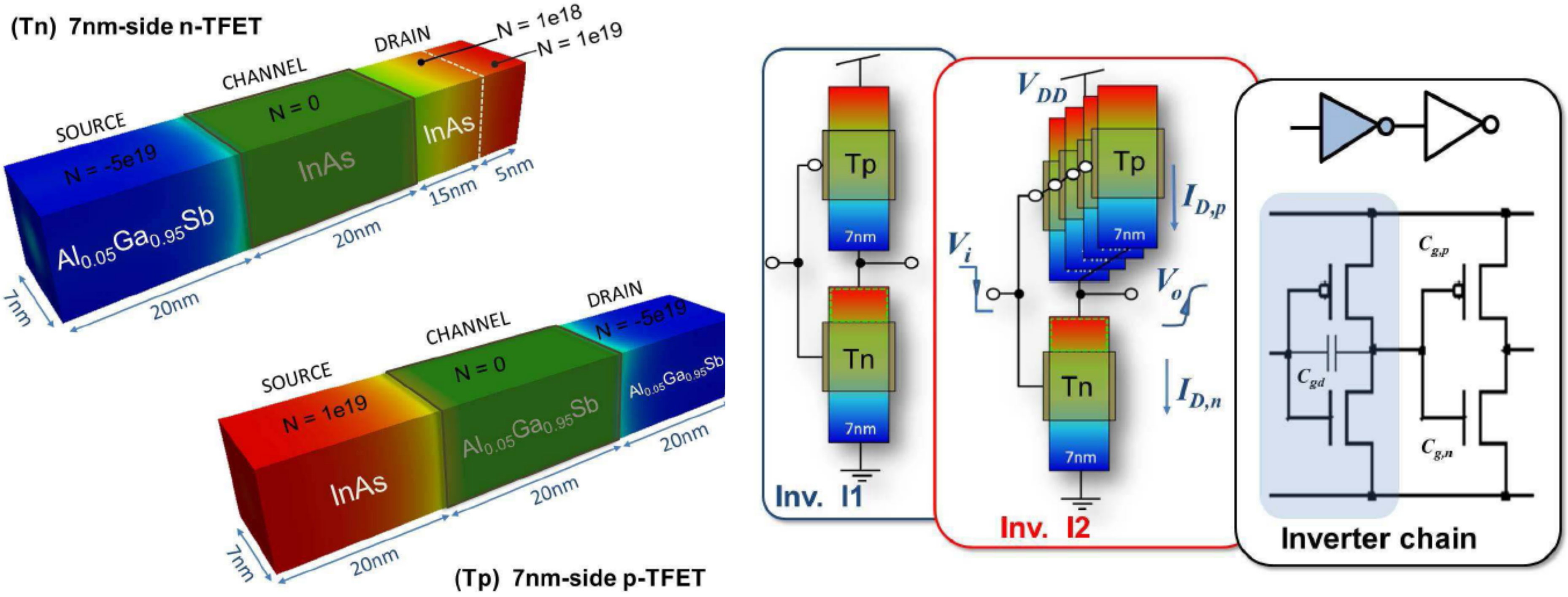
Experiments: Dewey et al., IEDM 2011





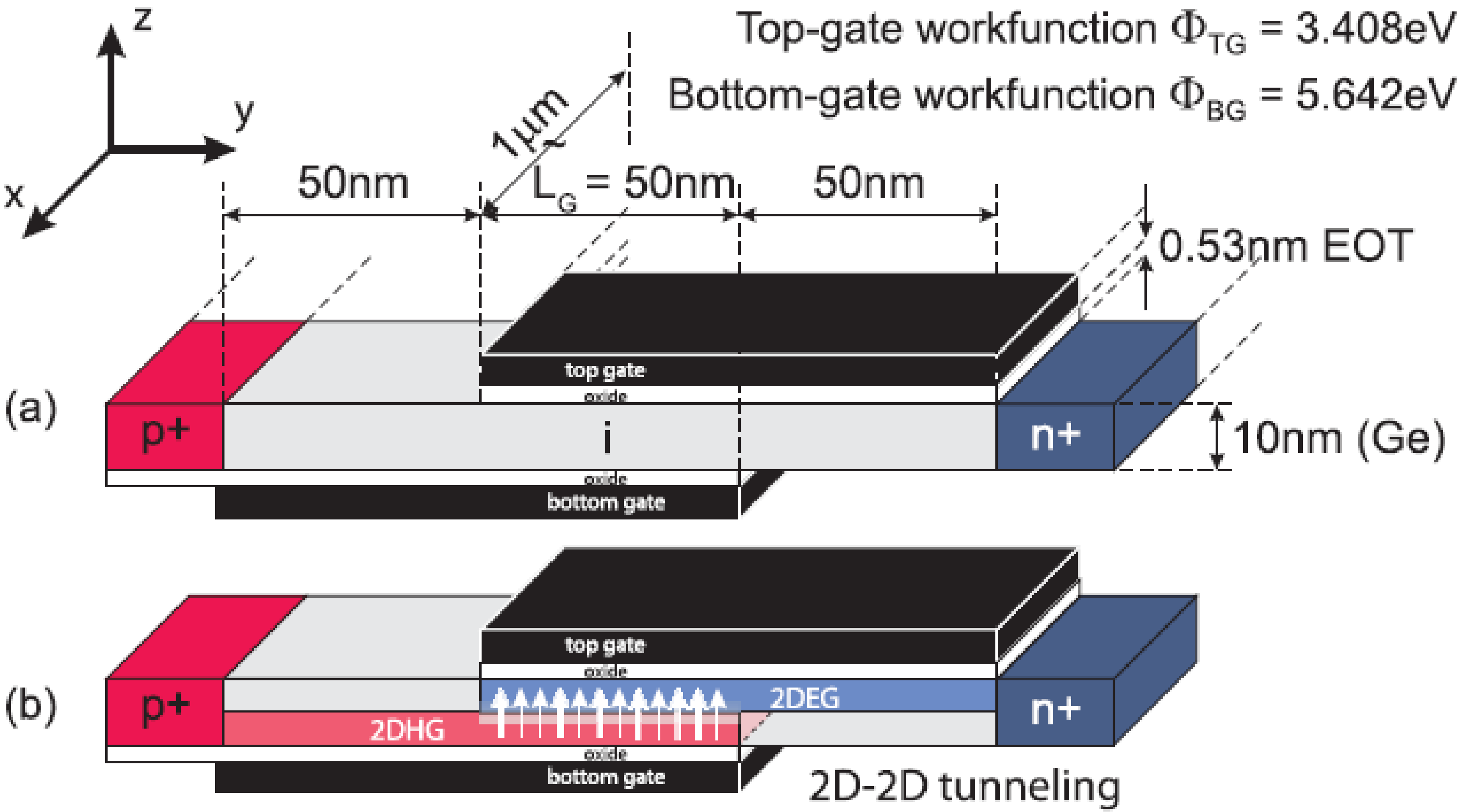
Inverters with InAs/AlGaSb TFETs

- **3D** Full-band quantum simulation with $V_{DD} = 0.25$ V
- **10x faster** than 10 nm FINFET for LOP (same I_{OFF})
- **100x faster** than 10 nm FINFET for LSTP (same I_{OFF})



E. Baravelli et al. IEEE TED 61, 473 (2014) - BOLOGNA

Ge e-h Bilayer TFET



- Tunneling occurs only when subbands are aligned
- Alper et al., TED 60, 2013 (UDINE+EPFL)

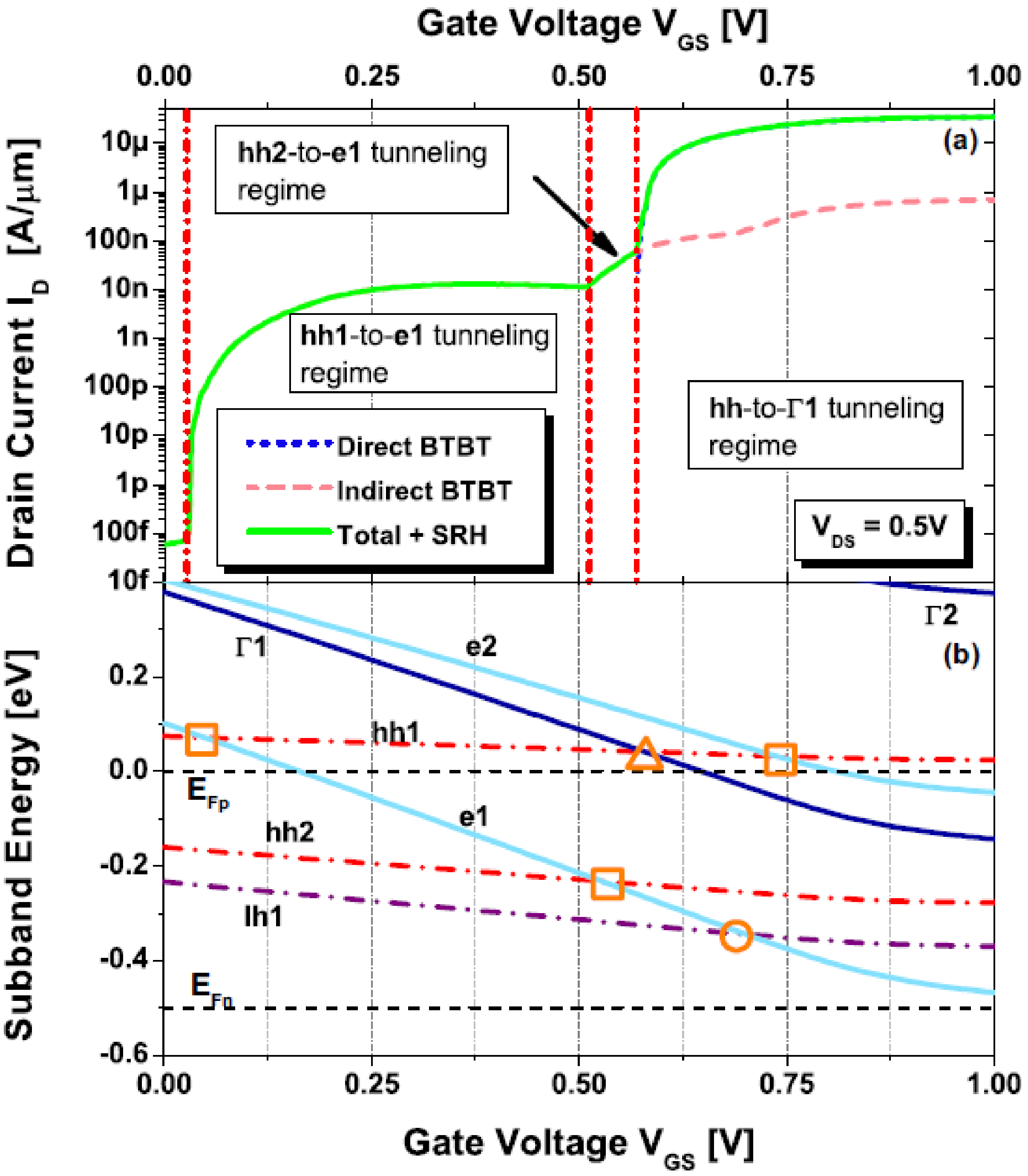
Ge e-h Bilayer TFET

- VB aligns with L → ph-assisted BTBT
- VB aligns with Γ → direct BTBT

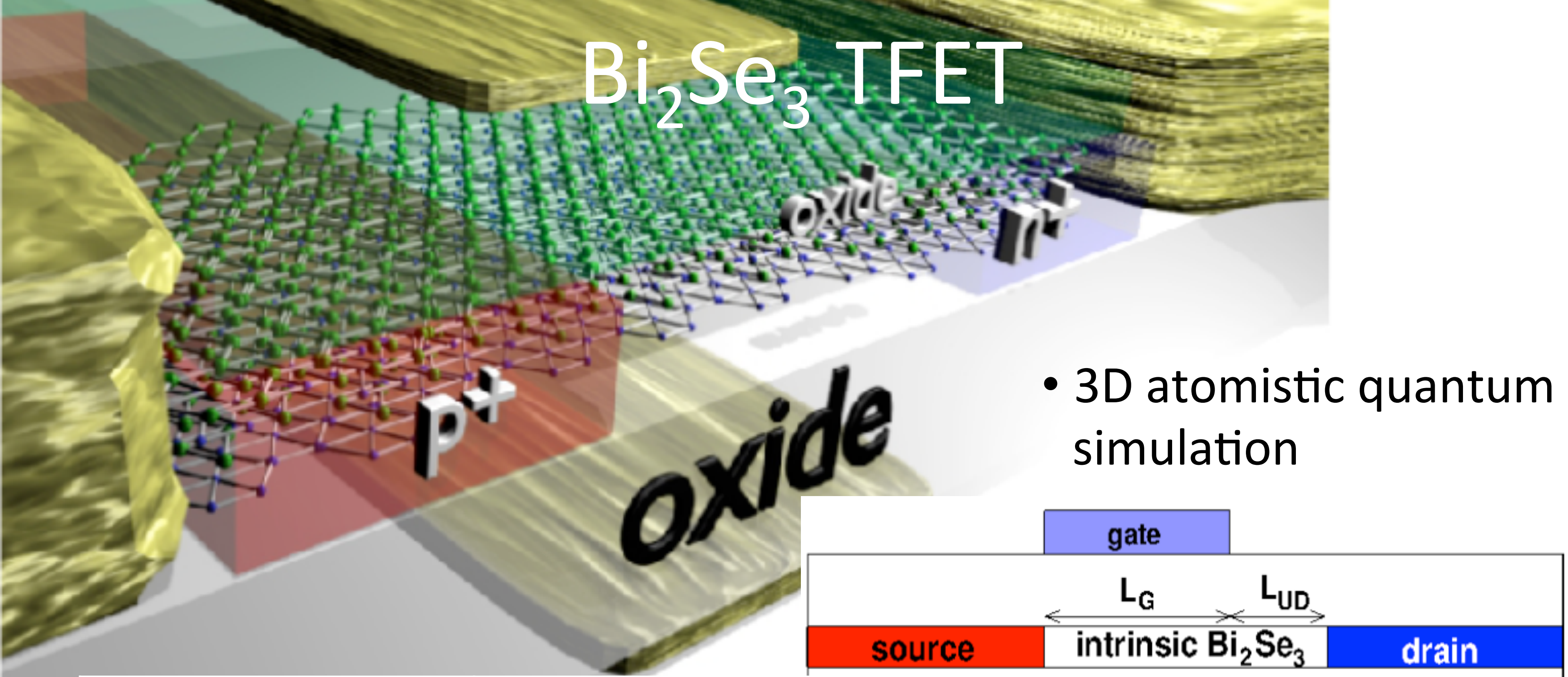
- steep transitions !

- on-current dominated by direct BTBT

Alper et al., TED 60, 2013 (UDINE+EPFL)



Bi_2Se_3 TFET



- 3D atomistic quantum simulation

	2014 LP MG MOSFET	InAs TFET	2QL BiSe TFET
Ch. length (nm)	13	15	10+15
V_{DD} (V)	0.57	0.3	**0.2**
I_{ON} (A/m)	794	15	48
DPI (fJ/µm)	**0.18**		**0.018**
$\tau = CV_{DD}/I$ (ps)	0.4		1.84

Q. Zhang et al - EDL 35, 129 (2014) - PISA

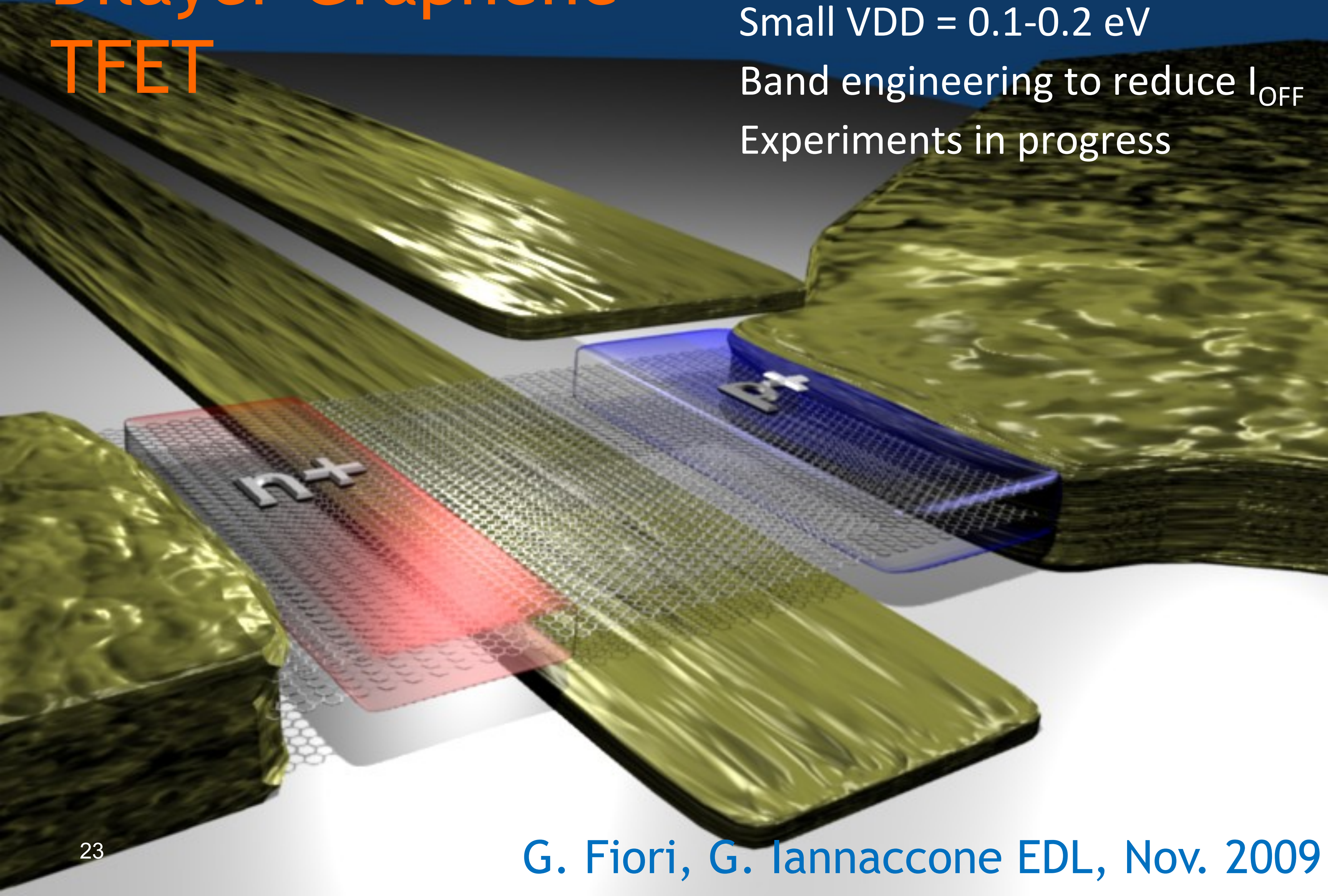
Bilayer Graphene TFET

Energy Gap ~0.2 eV

Small VDD = 0.1-0.2 eV

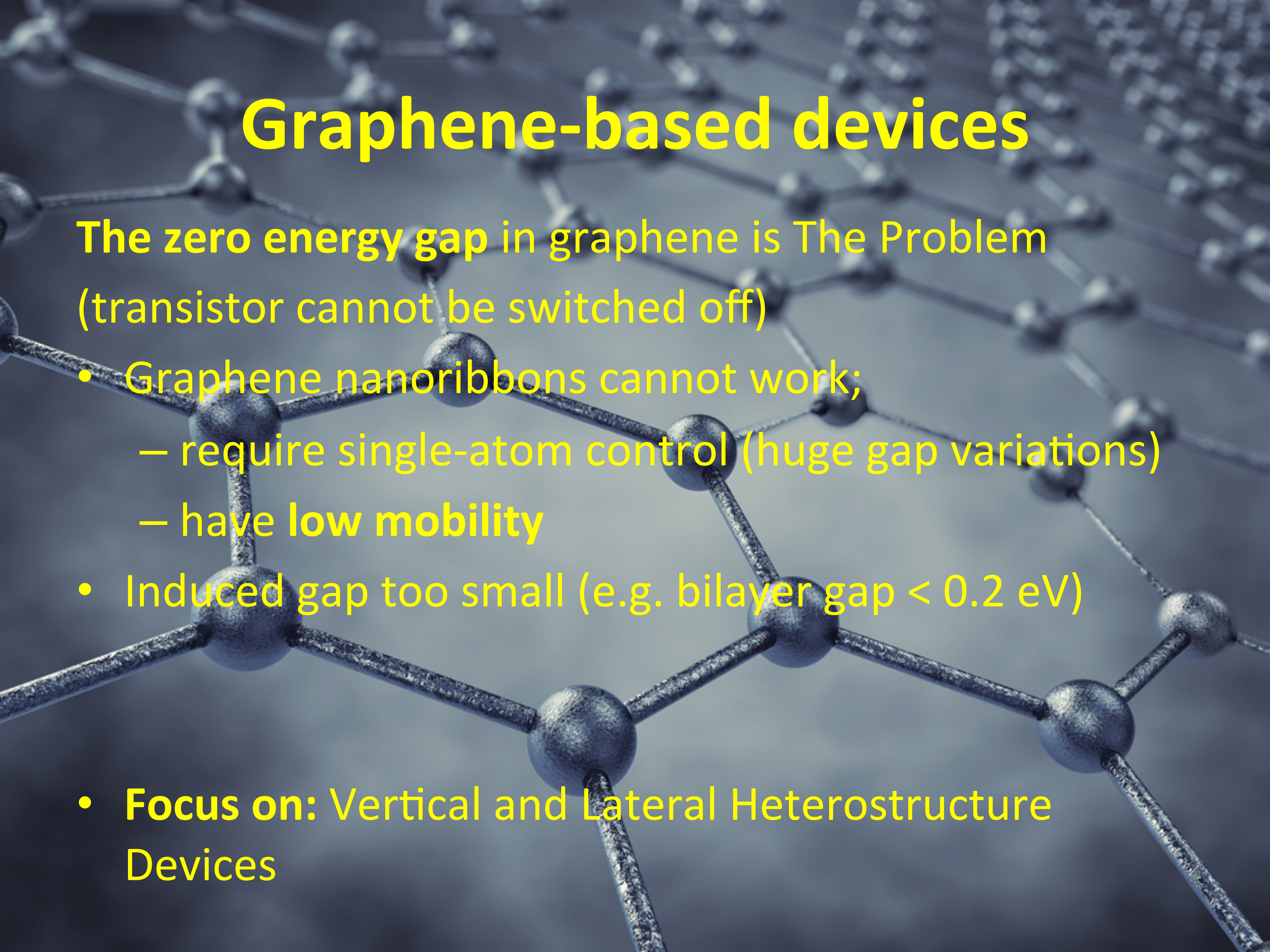
Band engineering to reduce I_{OFF}

Experiments in progress



G. Fiori, G. Iannaccone EDL, Nov. 2009

Graphene-based devices

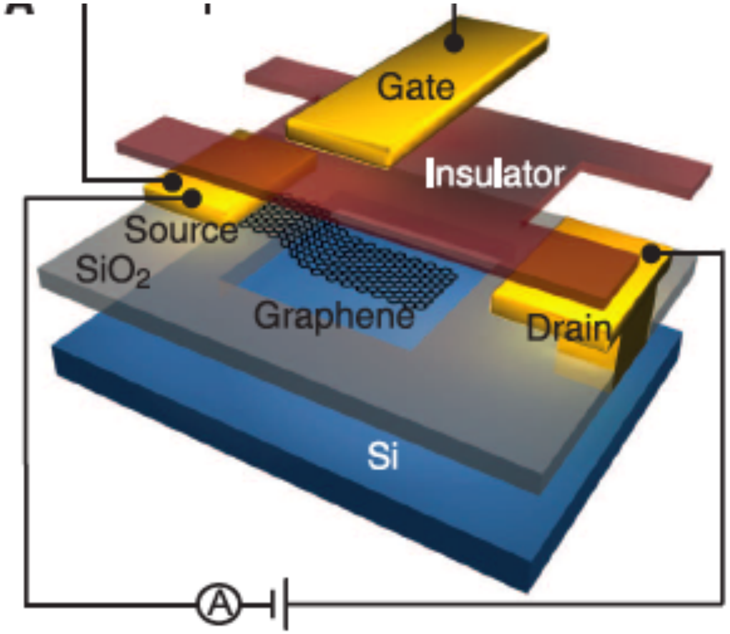


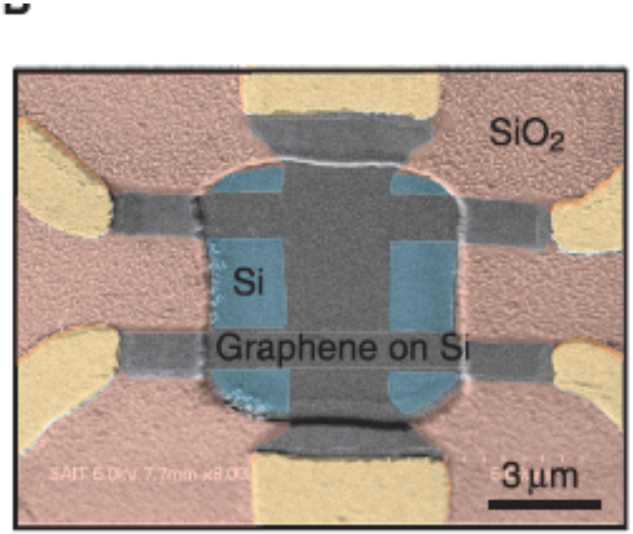
The zero energy gap in graphene is The Problem (transistor cannot be switched off)

- Graphene nanoribbons cannot work;
  - require single-atom control (huge gap variations)
  - have **low mobility**
- Induced gap too small (e.g. bilayer gap < 0.2 eV)

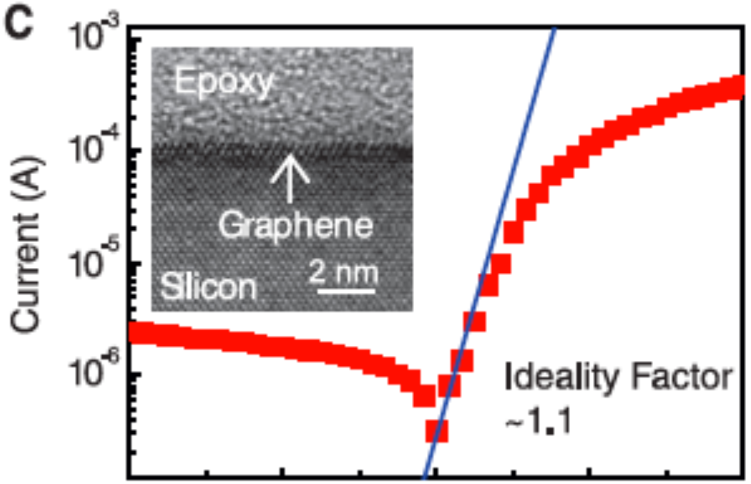
- **Focus on:** Vertical and Lateral Heterostructure Devices

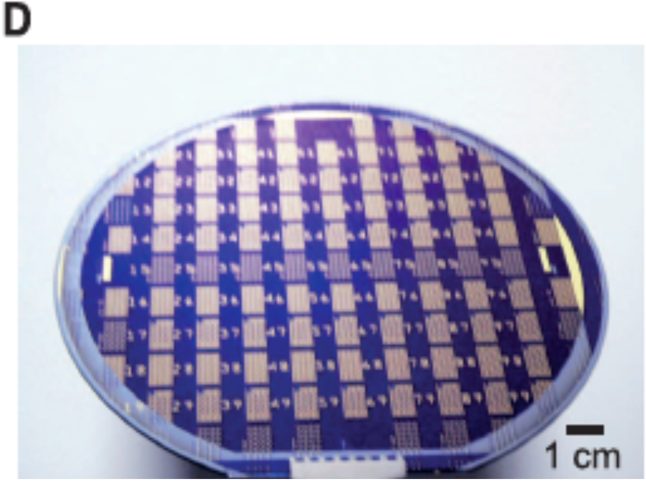
Graphene Barristor





K. Yang, Science 2012
(SAIT,Columbia U., Samsung)





NANO LETTERS

Letter

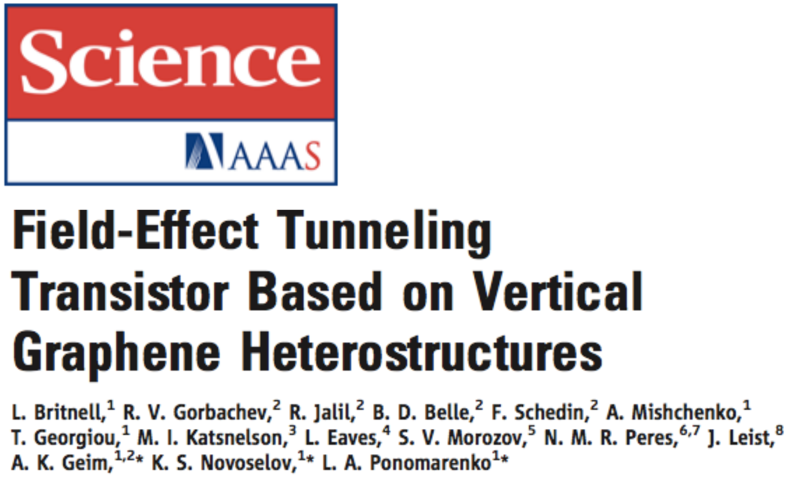
pubs.acs.org/NanoLe

Electron Tunneling through Ultrathin Boron Nitride Crystalline Barriers

Liam Britnell,[†] Roman V. Gorbachev,[‡] Rashid Jalil,[‡] Branson D. Belle,[‡] Fred Schedin,[‡] Mikhail I. Katsnelson,[§] Laurence Eaves,[‖] Sergey V. Morozov,[⊥] Alexander S. Mayorov,[†] Nuno M. R. Peres,[#,∇] Antonio H. Castro Neto,[∇] Jon Leist,[◆] Andre K. Geim,[†,‡] Leonid A. Ponomarenko,[†] and Kostya S. Novoselov*,[†]

Britnell et al. Nano Letters 2011

Britnell et al. Science 2011

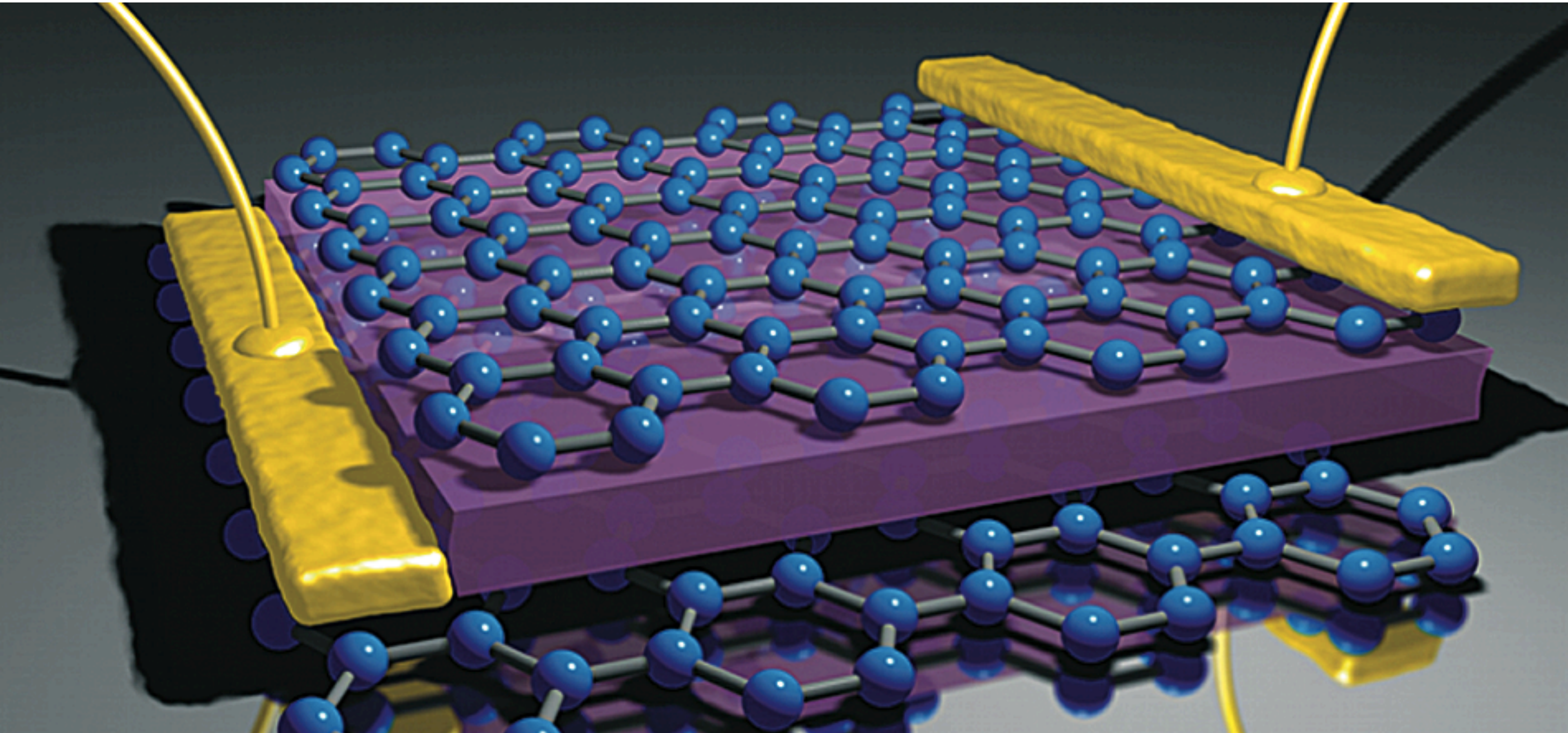


Science

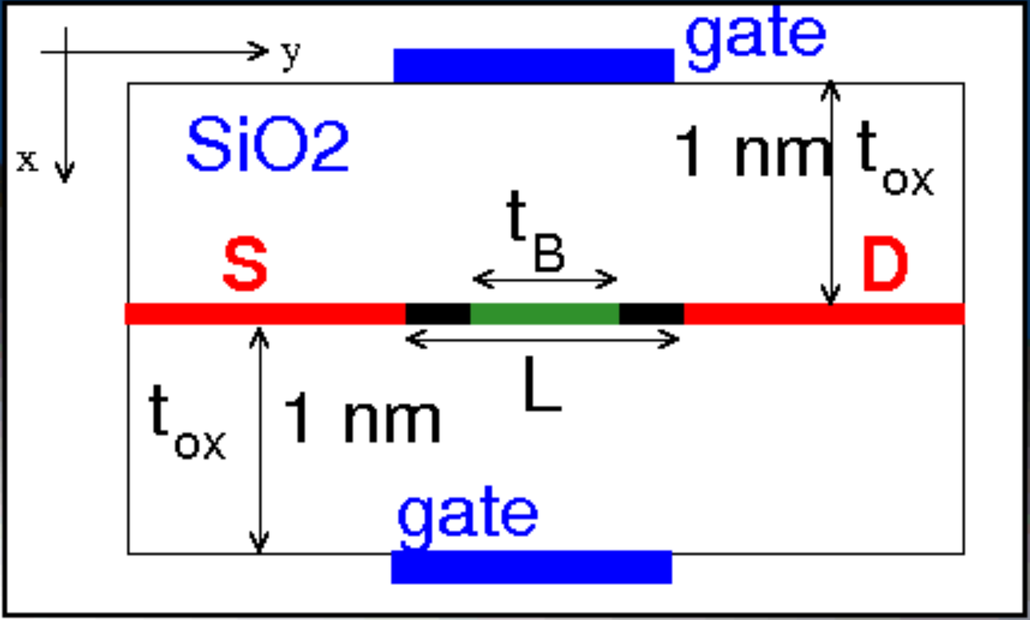
AAAS

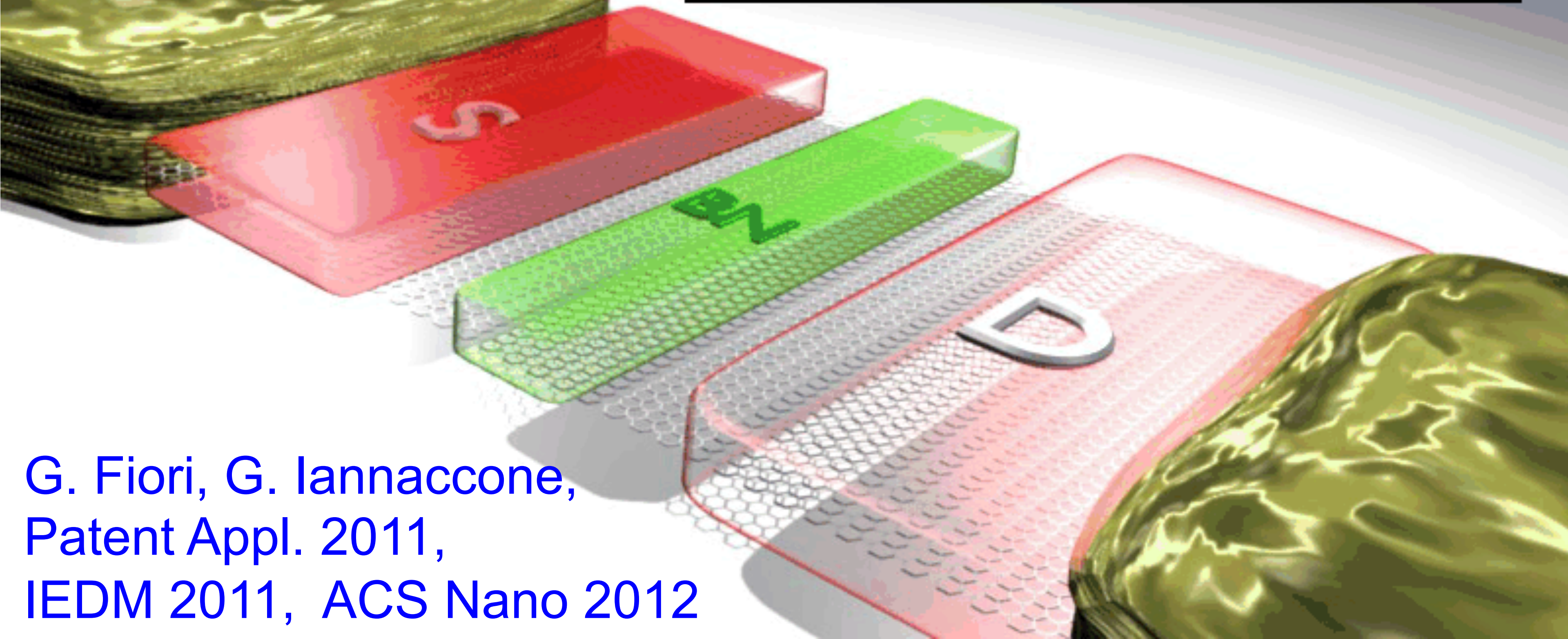
Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures

L. Britnell,[1] R. V. Gorbachev,[2] R. Jalil,[2] B. D. Belle,[2] F. Schedin,[2] A. Mishchenko,[1] T. Georgiou,[1] M. I. Katsnelson,[3] L. Eaves,[4] S. V. Morozov,[5] N. M. R. Peres,[6,7] J. Leist,[8] A. K. Geim,[1,2]* K. S. Novoselov,[1]* L. A. Ponomarenko[1]*



Lateral heterostructure FET

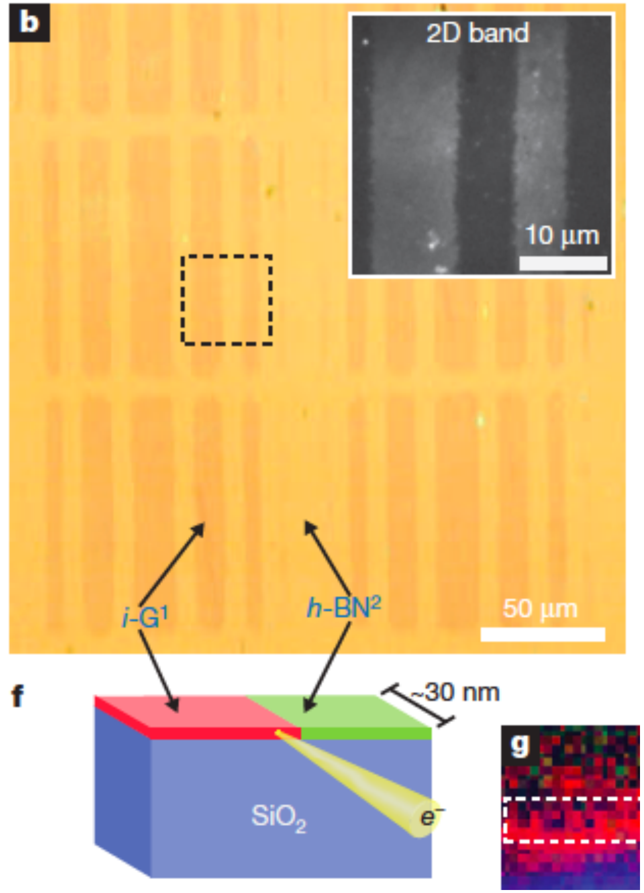


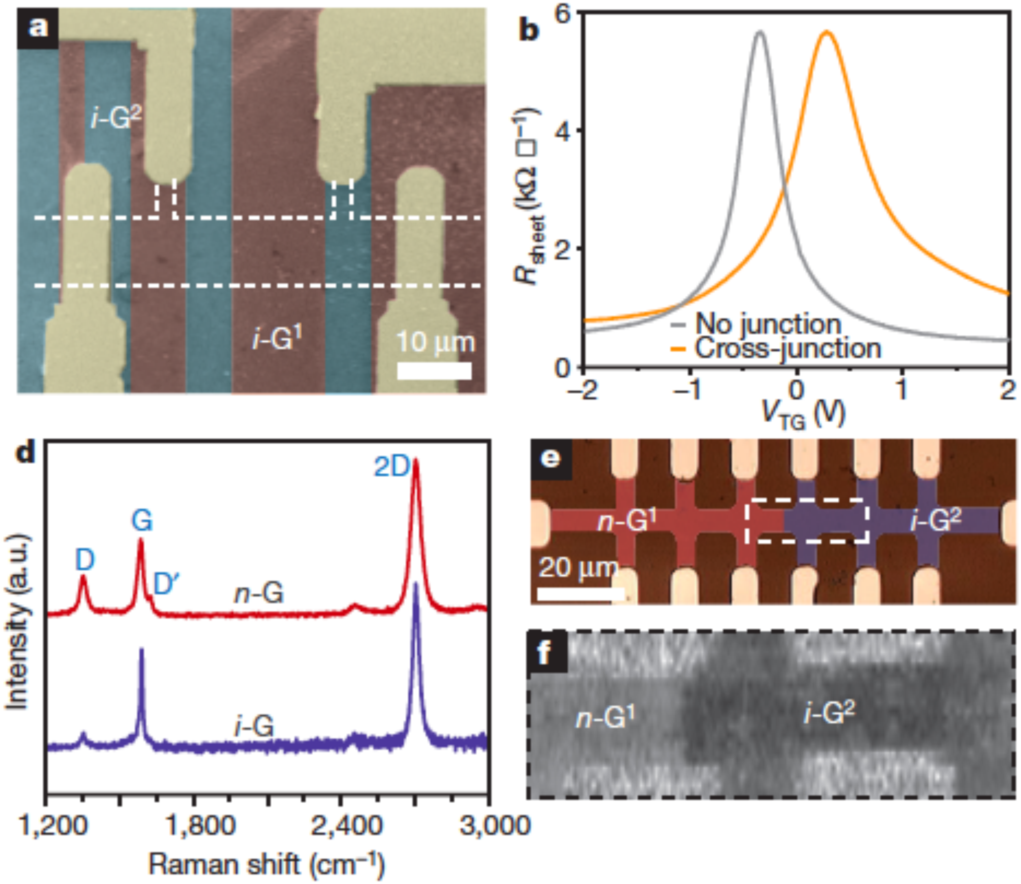


G. Fiori, G. Iannaccone,
Patent Appl. 2011,
IEDM 2011, ACS Nano 2012

Lateral G-BN Heterostructures

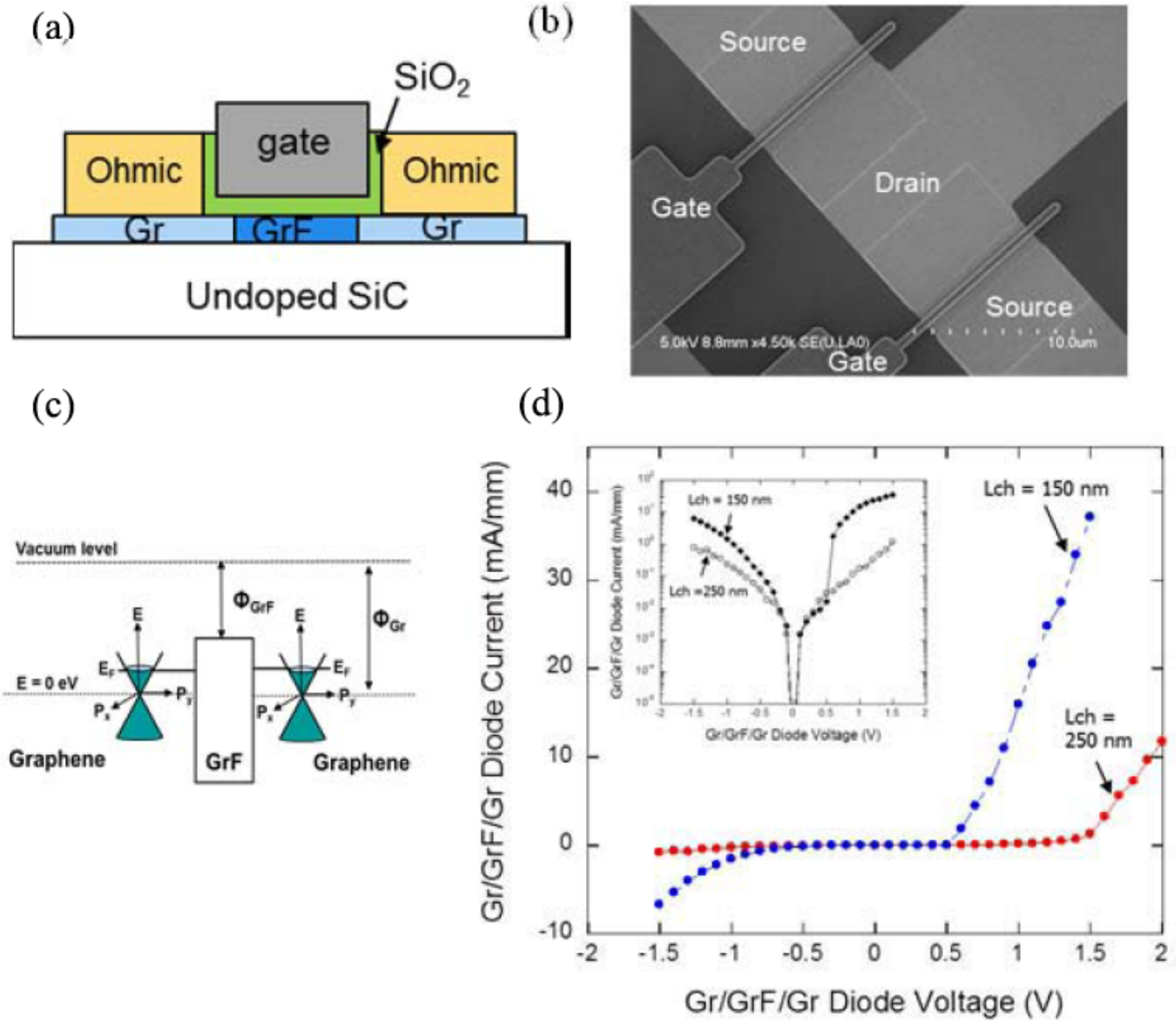
M.P. Levendorf
Nature 2012
(Cornell)





LHFET Experimental Demonstration

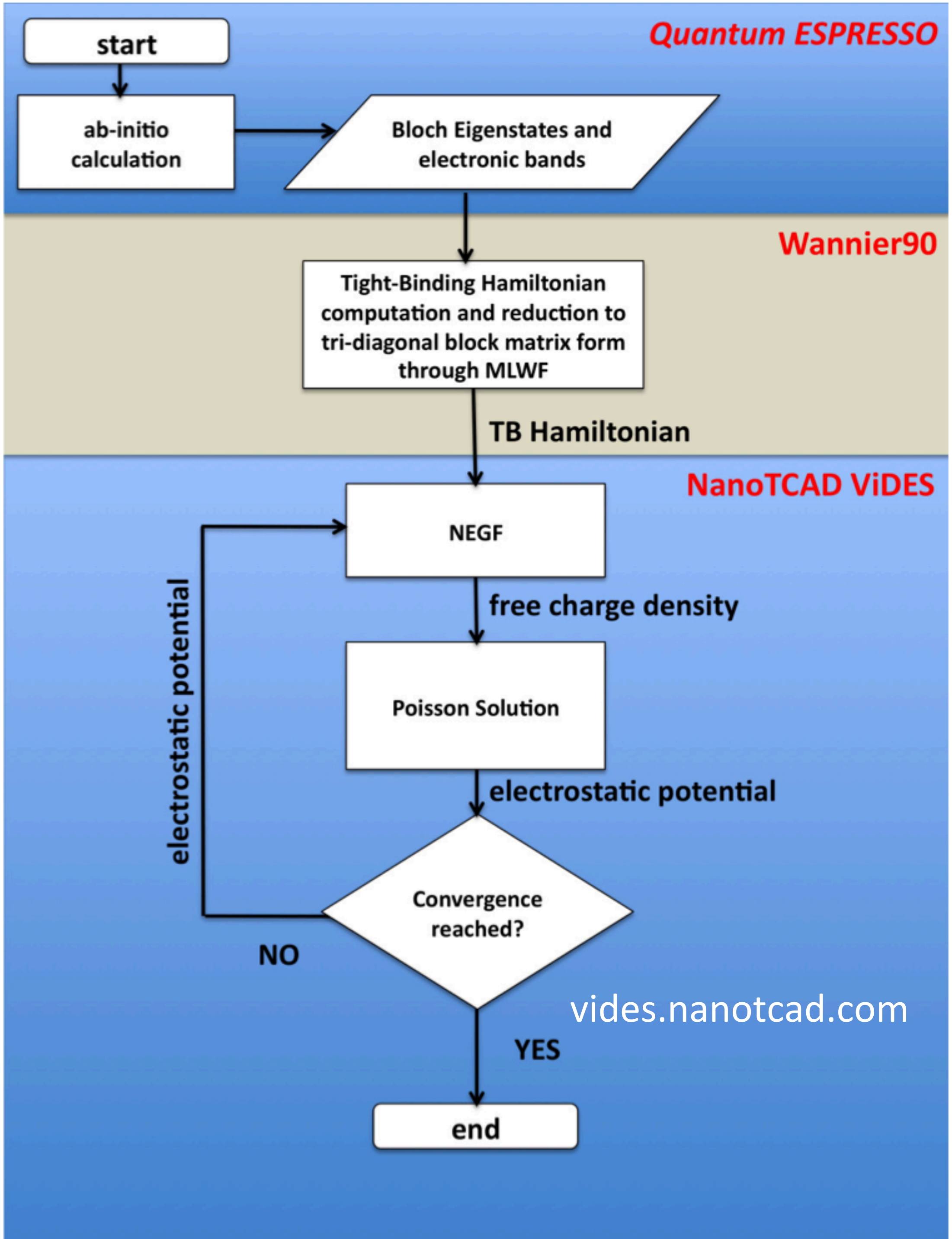
Moon et al. (HRL), EDL 34, 1190, 2013



Multi-scale Modeling

A multi-scale approach for the simulation of nanoscale devices with self-extraction of tight-binding parameters from ab-initio simulations

1. **DFT (Materials modeling)**
   Quantum Espresso
2. **Wannier 90**
3. **NEGF-TB**
   NanoTCAD ViDES



Quantum ESPRESSO

start

ab-initio calculation

Bloch Eigenstates and electronic bands

Wannier90

Tight-Binding Hamiltonian computation and reduction to tri-diagonal block matrix form through MLWF

TB Hamiltonian

NanoTCAD ViDES

NEGF

free charge density

Poisson Solution

electrostatic potential

Convergence reached?

NO

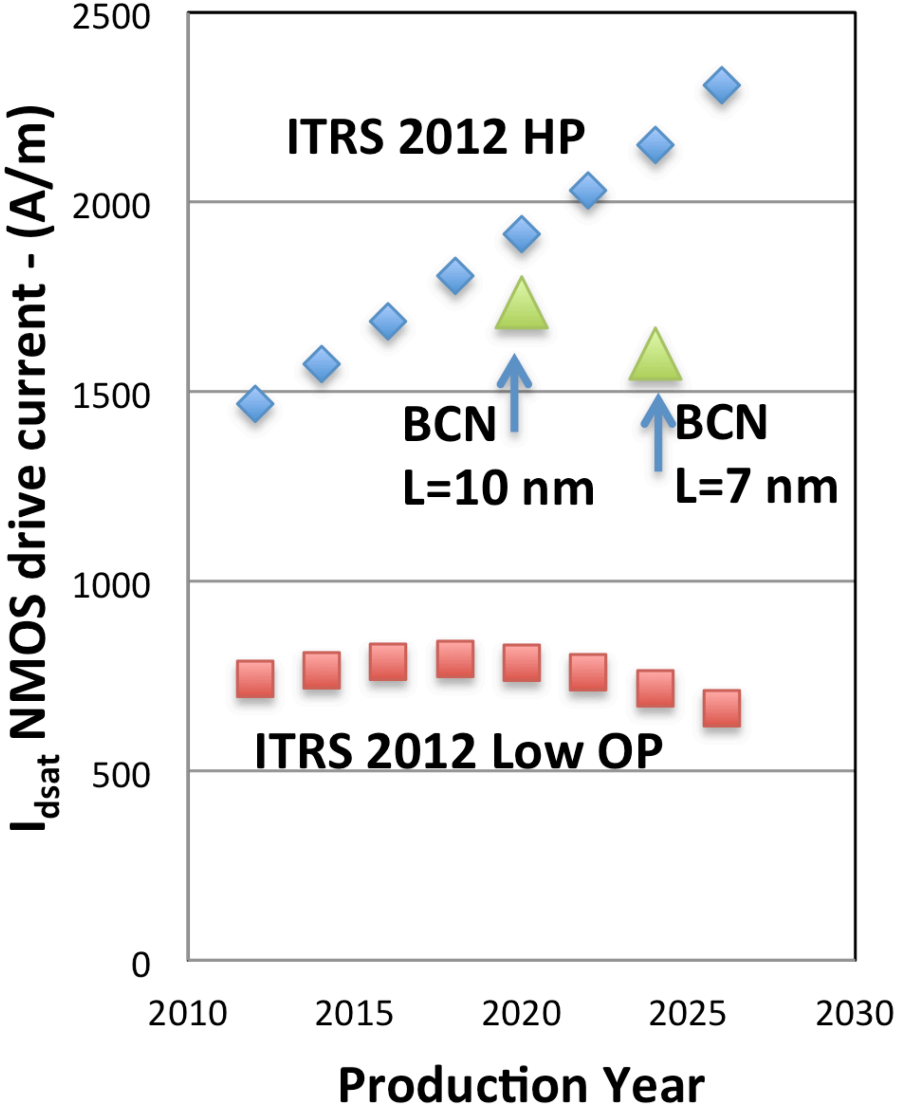
electrostatic potential

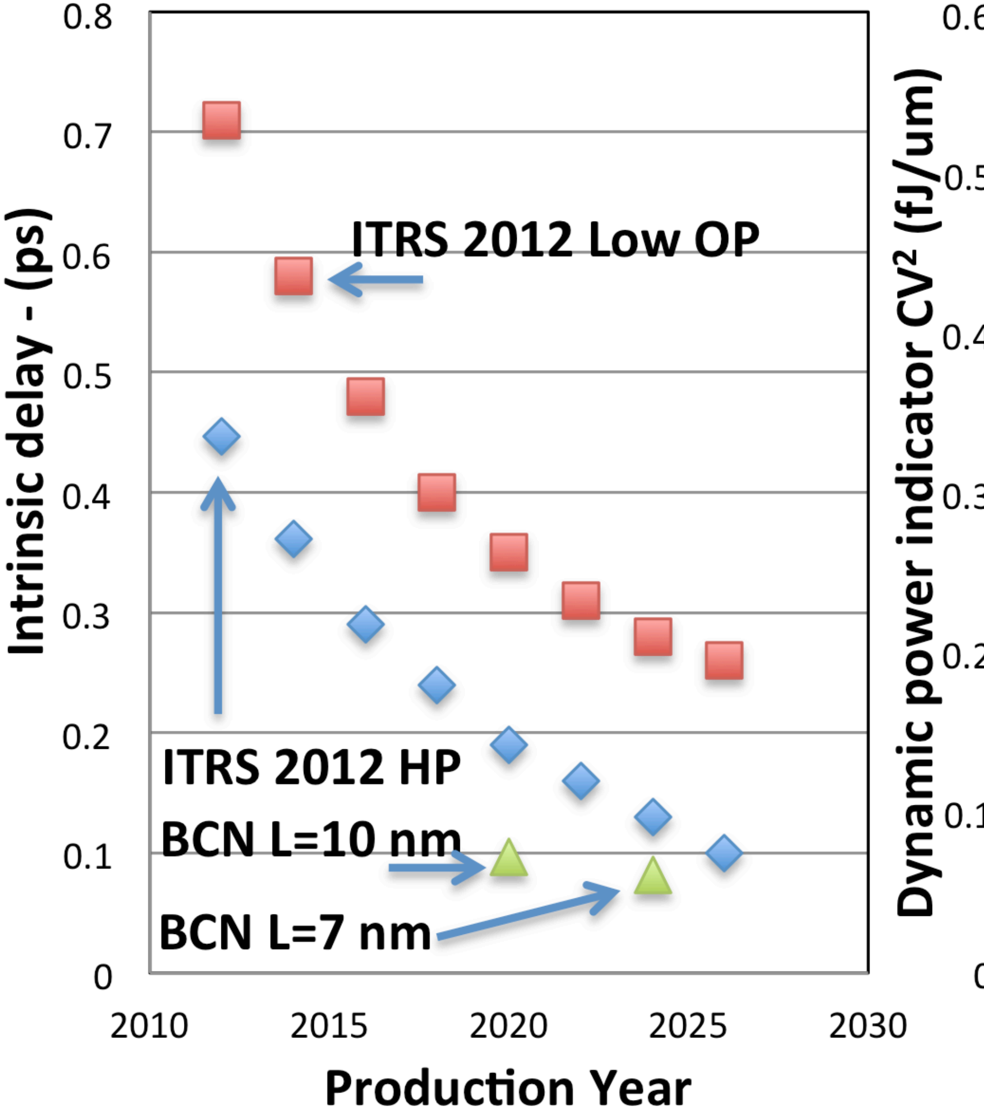
YES

end

vides.nanotcad.com

Graphene LHFET – vs ITRS 2012

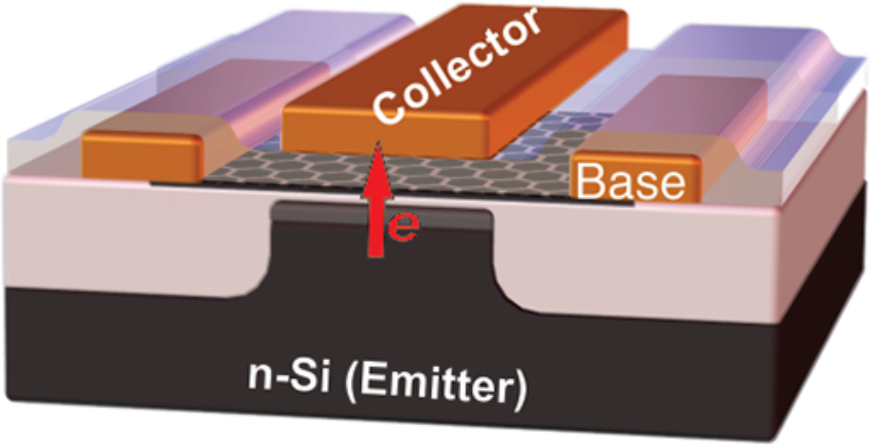


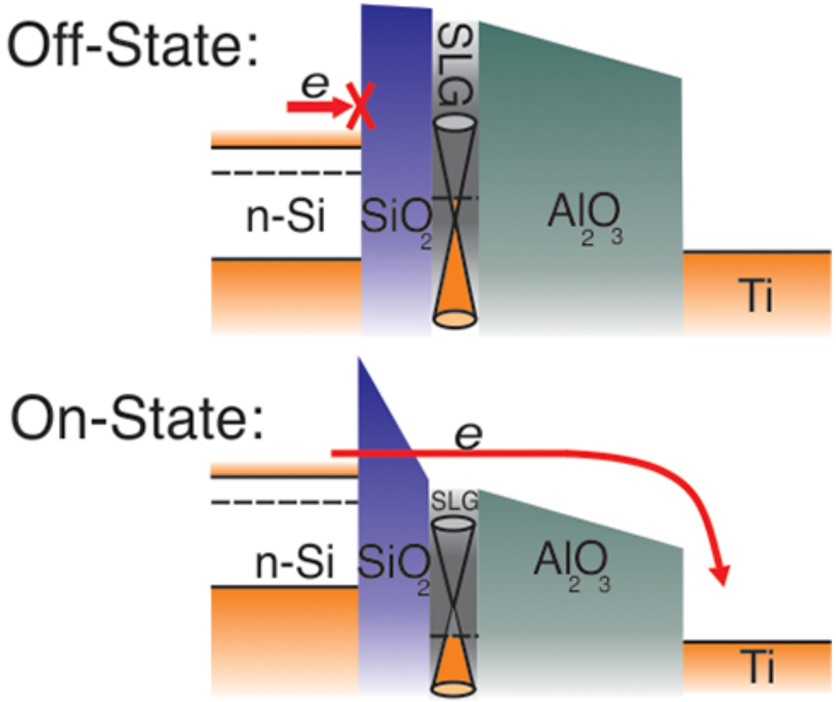


VHFET: τ = 625 ps **Barristor:** τ = 160 ps

Graphene-base hot electron transistor

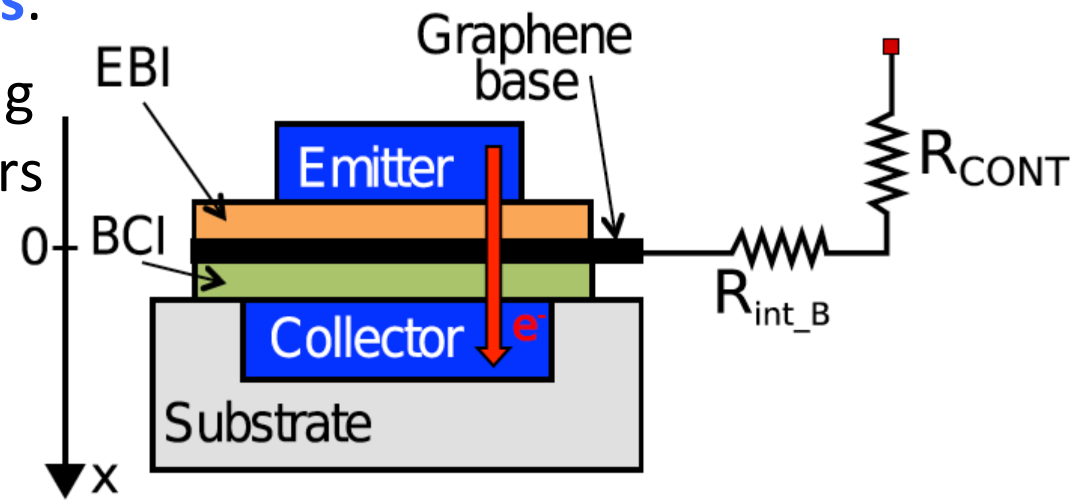
S. Vaziri et al.
(KTH,U. Siegen, IHP)
Nano Letters 2012





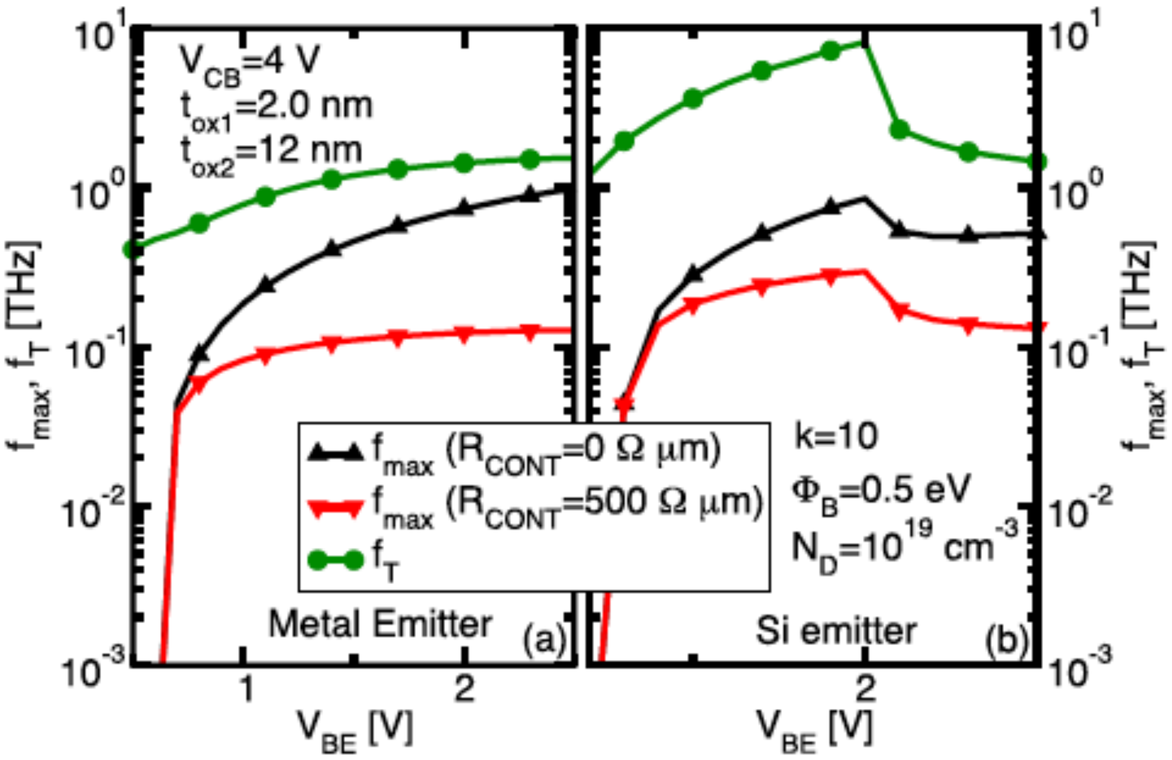
Optimized design of the GBT

- 1D model for GBT electrostatic and currents
- **Self consistent Electrostatics**:
- **Tunnelling currents** including Energy distribution of carriers in emitter and base accounted for
- **Cut-off frequency (f_T)** estimated with quasi-static approach
- **Montecarlo model for the simulation of base current in GBTs**



S. Venica et al. TED 61, 2570 (2014) - UDINE

GBT optimization



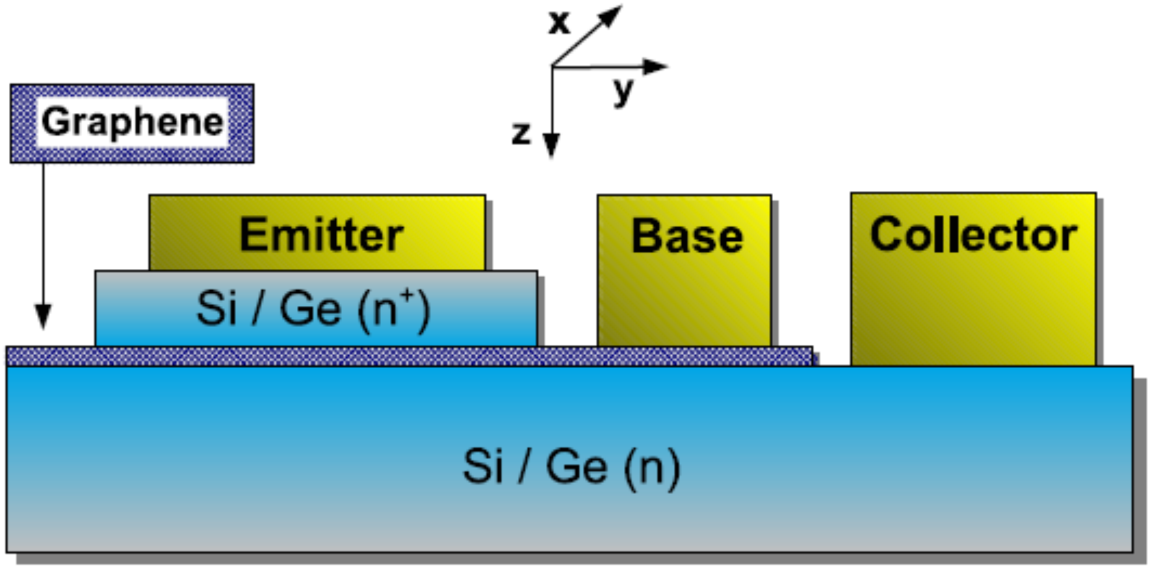
	DEV. 1	DEV. 2
Emitter	Si N_D=10^{19} cm^{-3}	Ti Φ_{M1}=4.33 eV
EBI	**Ta_2O_5**	**SiCOH**
BCI	**Ta_2O_5**	**SiCOH**
k [ε_0]	25	2.5
Φ_{B1} [eV]	0.36	0.53
Φ_{M2} [eV]	4.33	4.33

- **THz operation possible**
- Si emitter GBT → Si band bending lowers EBI → Larger band bending for larger k value
- Metal emitter GBT → lower k results in lower capacitance

S. Venica et al. TED 61, 2570 (2014)

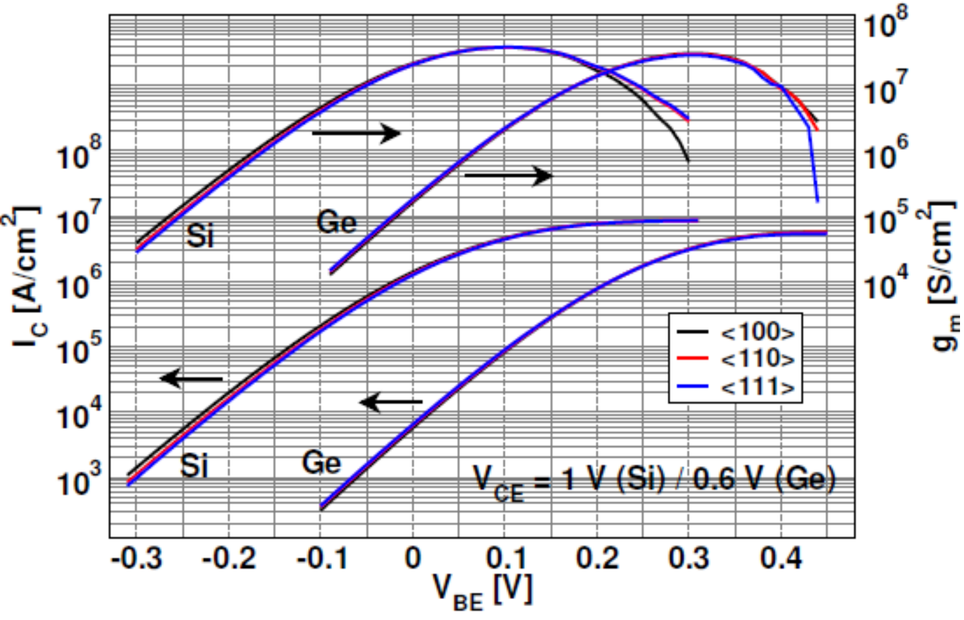
Graphene Base Heterojunction Transistor (GBHT)

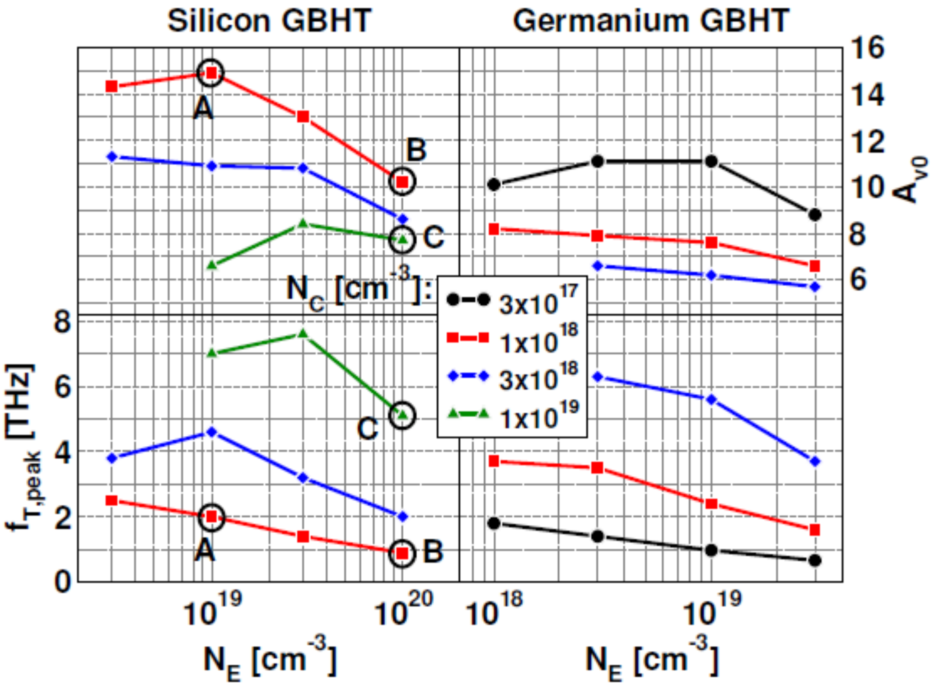
- Impact of different orientations and materials (Si/Ge)
- Sensitivity to doping concentrations
- Effect of graphene base resistance (f_{MAX})
- Inclusion of ionized impurity scattering in Si



V. Di Lecce et al. , TED60, 4263 (2013) - BOLOGNA

GHBT Impact of doping, materials

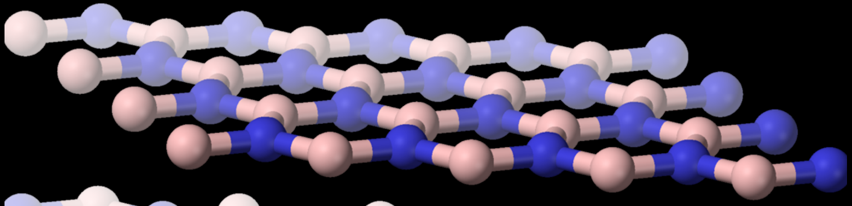


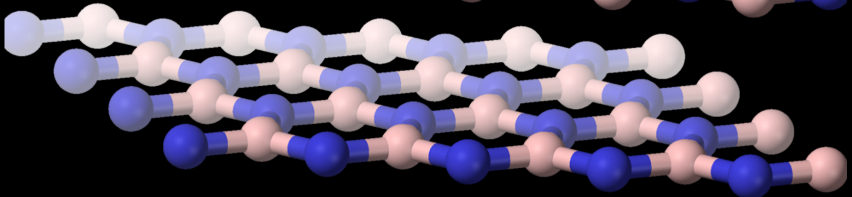


- **THz Operation Possible**
- Si and Ge provide comparable performance

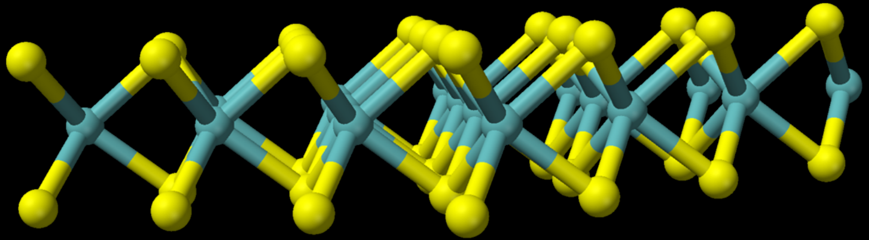
V. Di Lecce et al. , TED60, 4263 (2013)

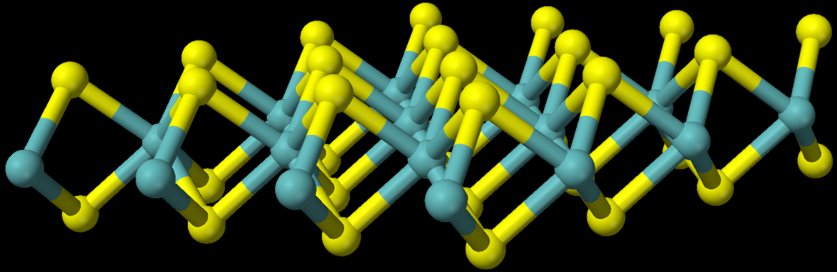
Other 2D materials





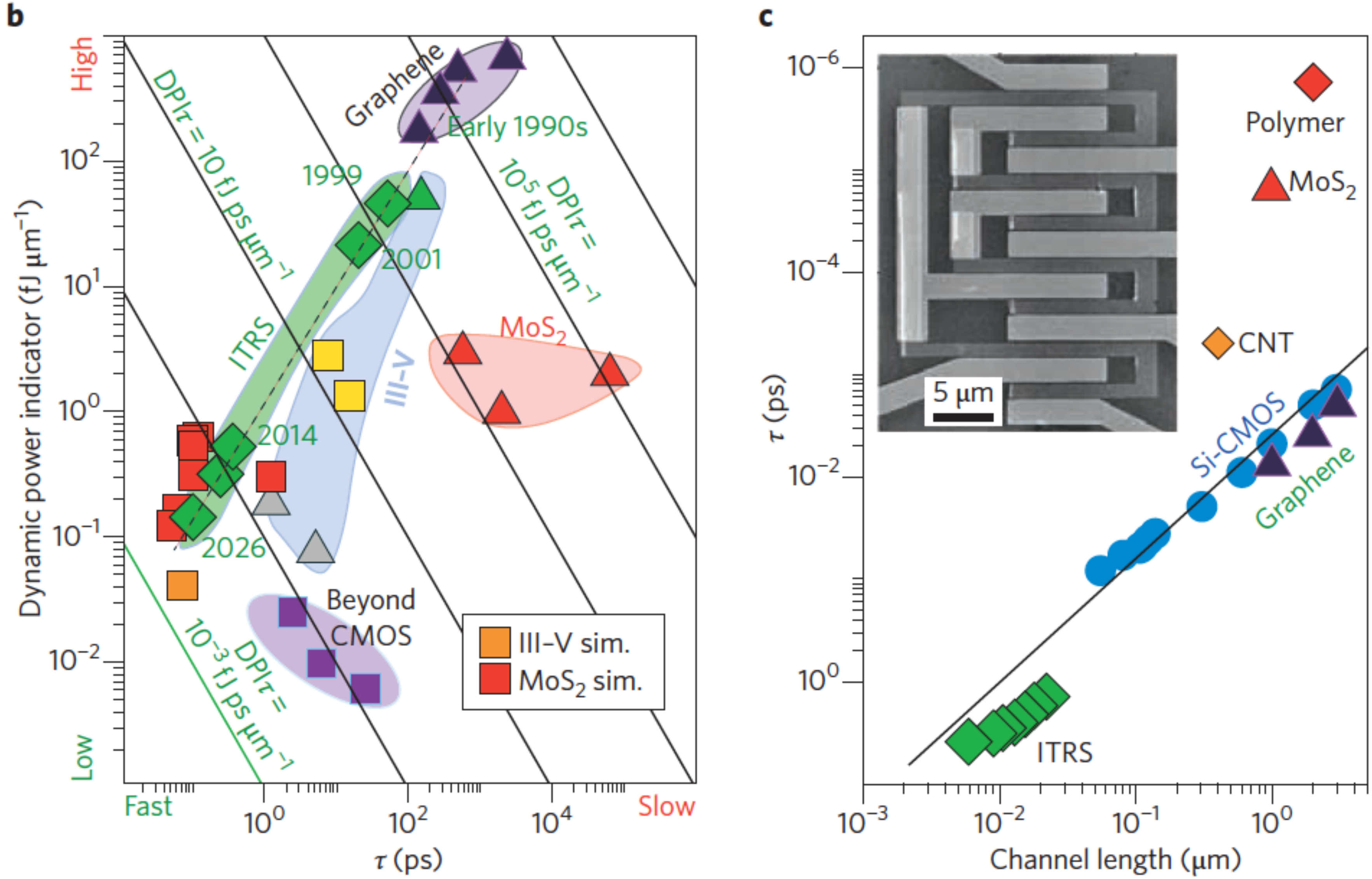
Boron Nitride





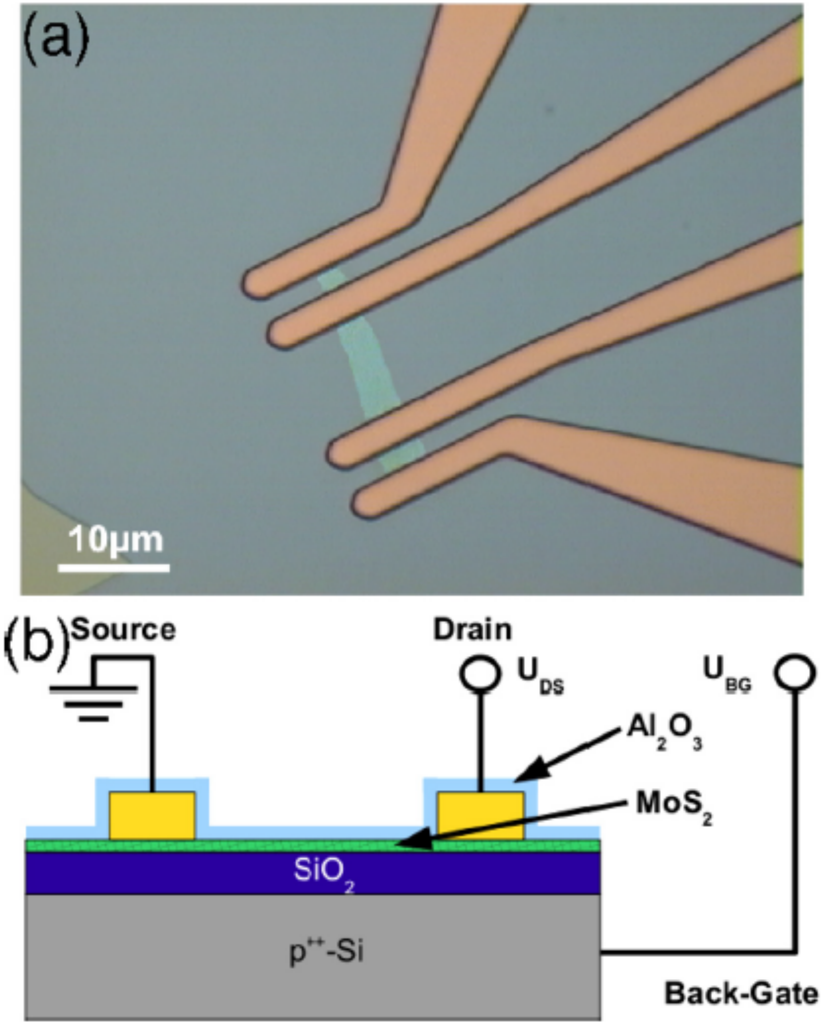
Molybdenum disulfide

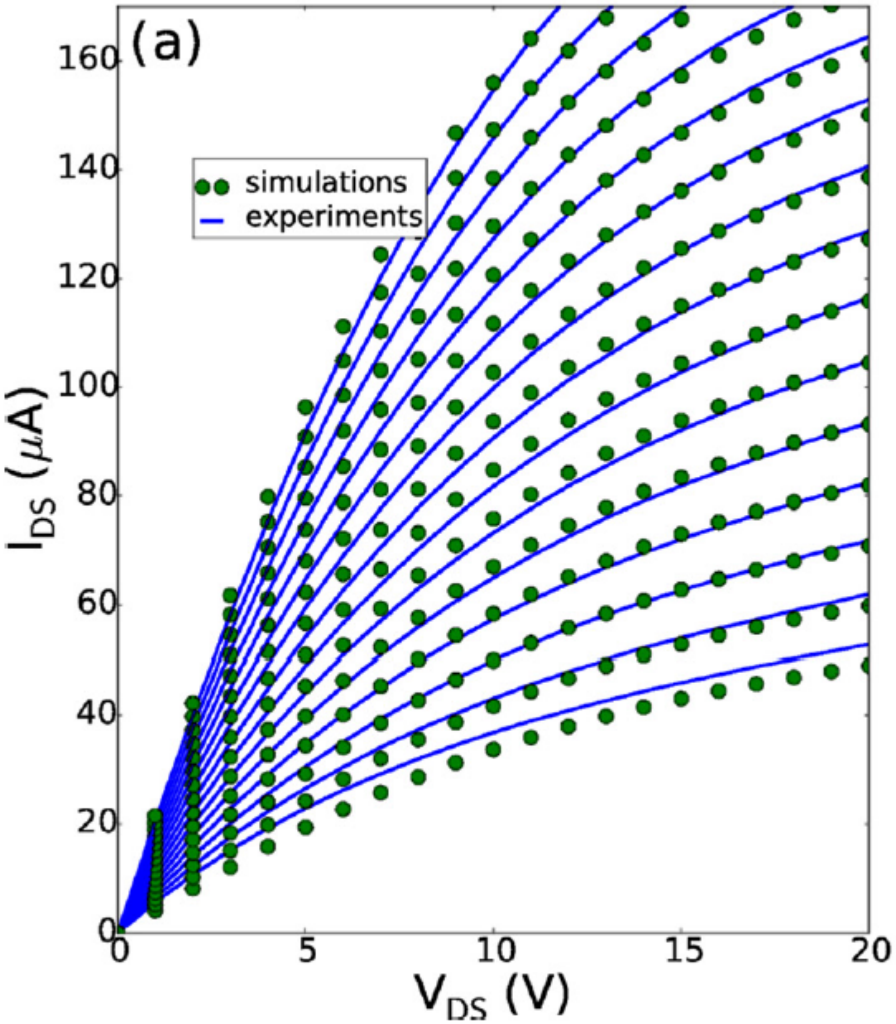
Next – other 2D materials ?



G. Fiori et al. Nature Nanotechnology, to appear 2014

Velocity saturation in MoS_2





G. Fiori et al., APL, 103, 233509, 2013 – Pisa and AMO

All in "Beyond CMOS"

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Thank you