Attività IUNET nell’area “More Moore”

Luca Selmi

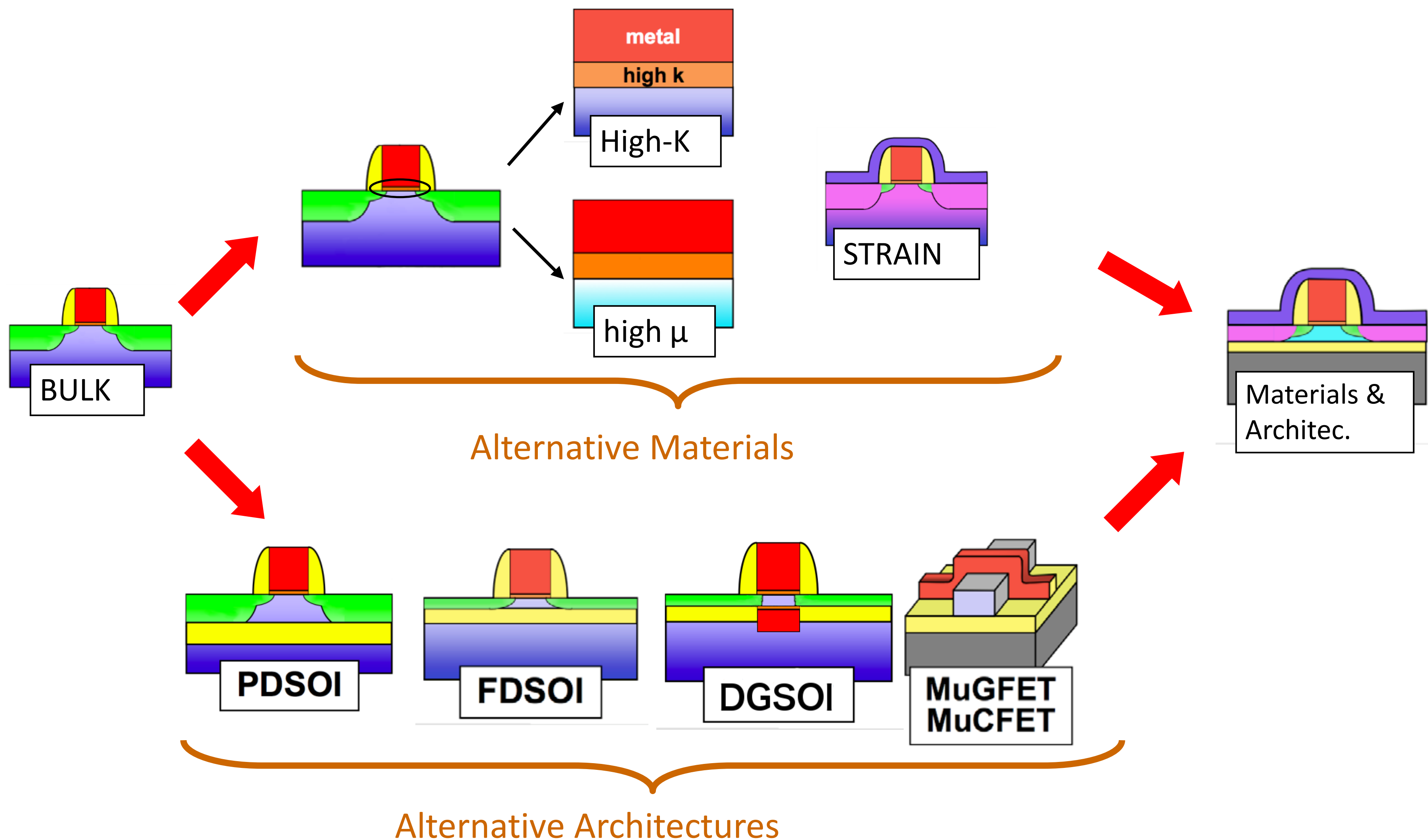
Third IUNET Day – Bologna, 18.9.2014

European Nanoelectronics Initiative Advisory Council (ENIAC)

- Research Priorities according to the Strategic Research Agenda:
  - More Moore
  - More than Moore
  - Heterogeneous Integration
  - Beyond CMOS
  - Design Automation
  - Equipment and Materials

- Capturing innovations and organizing European research activities in the rapidly evolving field of nanoelectronics

From Dennard's to equivalent scaling: Technology Boosters in the ITRS 2005



Fully Depleted FET architectures

Silicon On Insulator (SOI) → FinFET → Omega FET → Gate All Around (GAA) FET

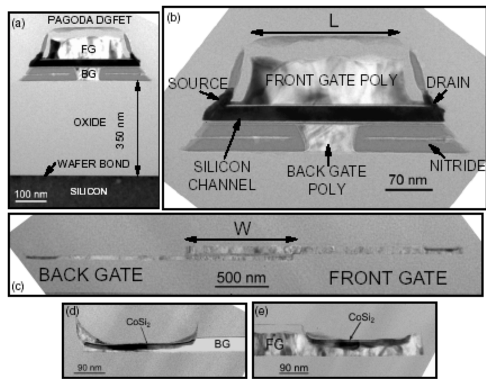


Fig. 8. TEM images of the PAGODA DGFET. (a) Full structure shows the bonded interface 350nm below the device. (b) Main cross section shows gate stack, silicided S/D silicon sidewalls, and undercut BG with nitride fill. This particular device had especially large undercut. (c) Cross section through gates, where sandwiched region (FG/channel/BG) is the device width, W. (d,e) Individual silicided contacts to front and back gates.

IBM: PAGODA

K.W.Guarini et al., IEDM 2001

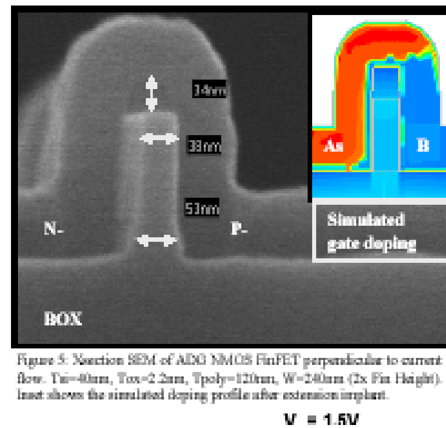


Figure 5: Xsection SEM of ADG NMOS FinFET perpendicular to current flow. Tsi=40nm, Tox=2.2nm, Tpoly=120nm, W=240nm (2x Fin Height). Inset shows the simulated doping profile after extension implant.

IBM: FinFET

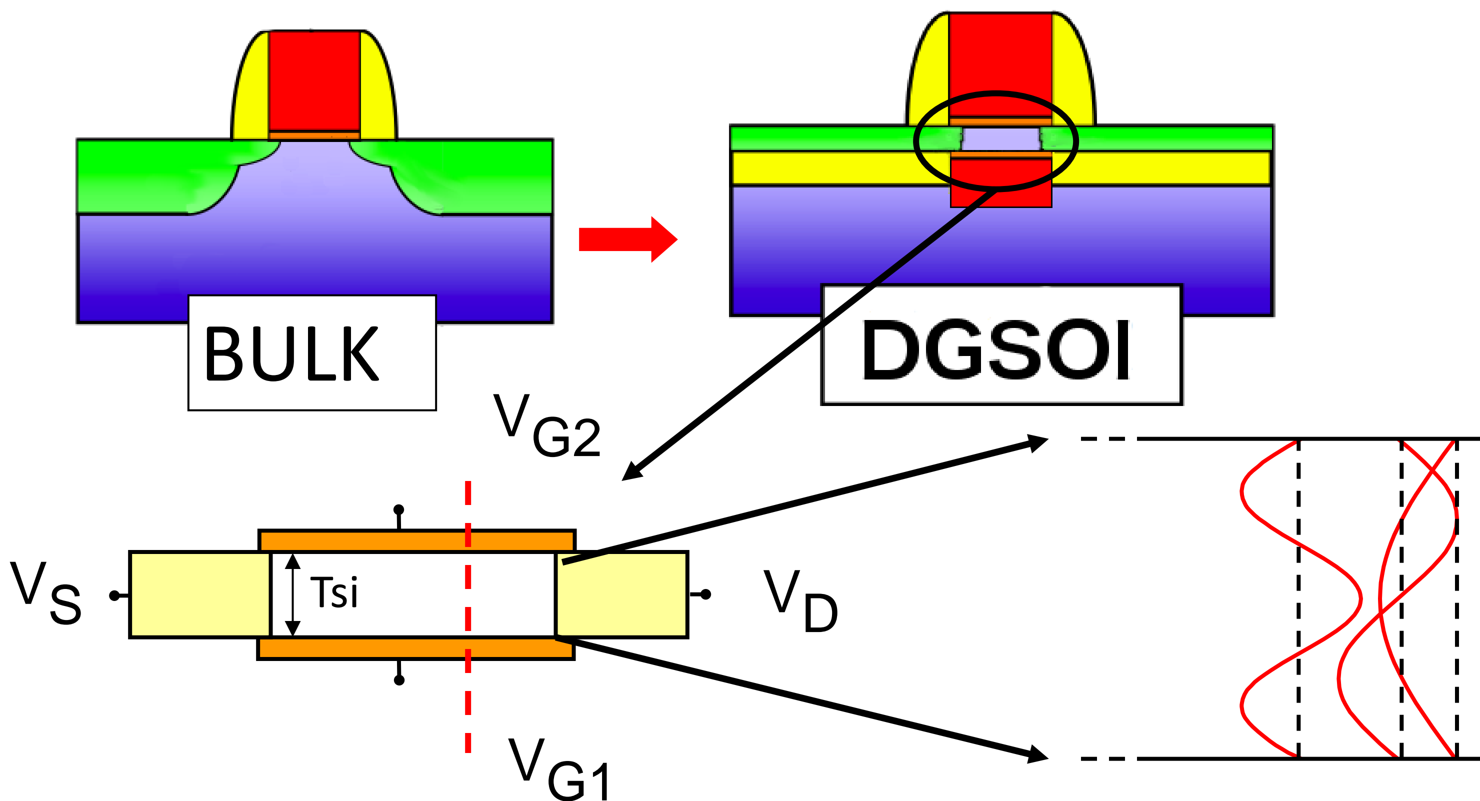
J.Kedzierski et al., IEDM 2001

Challenges and Opportunities

- Large number of technology options
- «Predictive» modeling needed by industry in new and unexplored fields
- Understanding of the underlying physics
- Expected feedback to companies and research centers

For the first time since many years industry was again looking at modeling and simulation as critically relevant activities

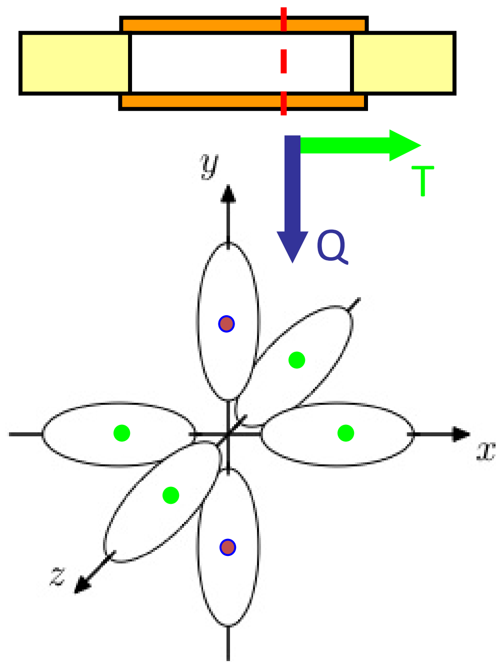
From bulk to FD UTB (SOI)

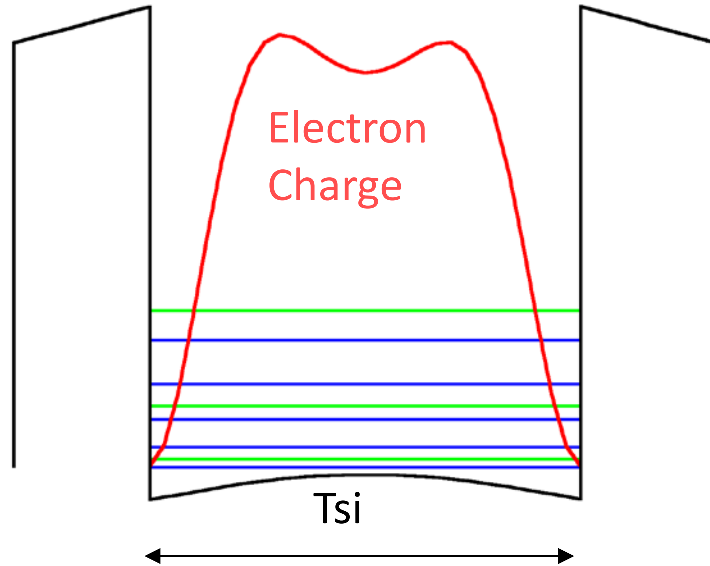


$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2}+U(x)\right]\psi(x)=E\psi(x)$$

A 2D carrier gas

Vertical quantum effects





QE on Electrostatics

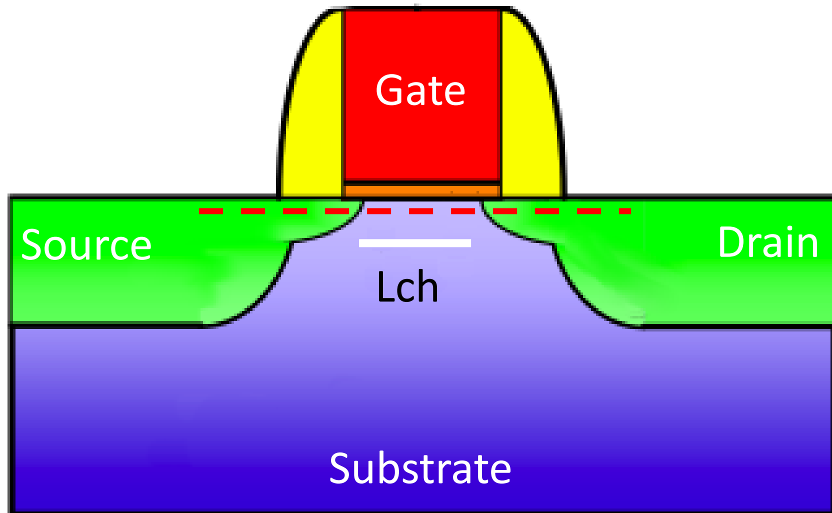
Quantum effects alter the effective transport mass of electrons

Quantum effects complicate the scattering theory!

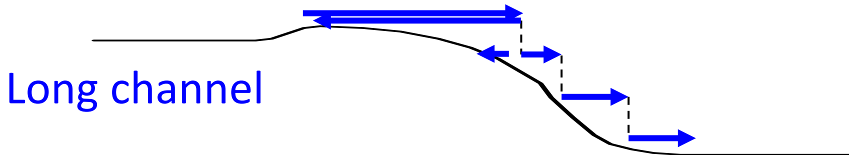
QE on Transport Properties

All bulk material properties are affected by device architecture and bias and <u>should be recomputed on a case by case basis</u>

Quasi-Ballistic transport



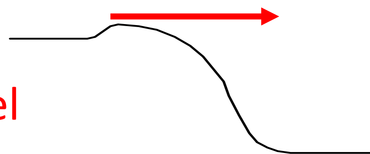
The channel length Lch is nowadays comparable to the carrier Mean-free-path



Long channel

Quasi equilibrium distribution in the channel: Drift-Diffusion

$$I_{DS} = \left[\frac{W}{L}\right] \frac{\mu_{eff} C_{ox}}{2} (V_{DD} - V_T)^2$$

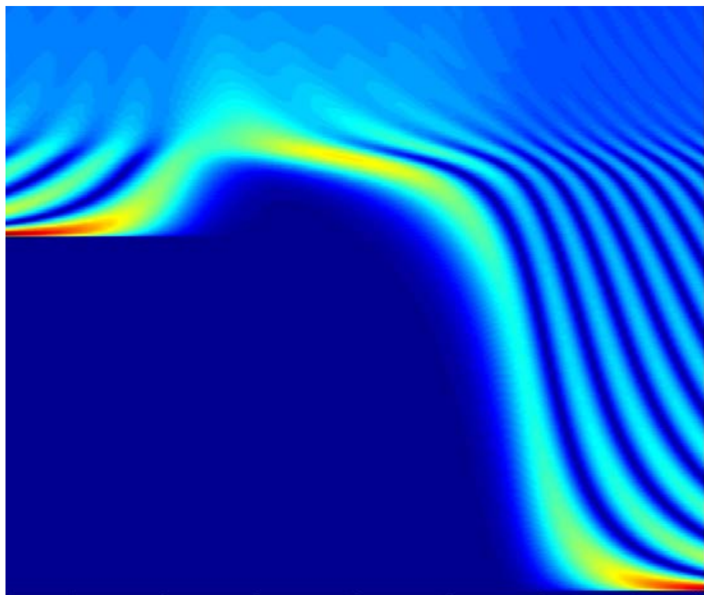


Short channel

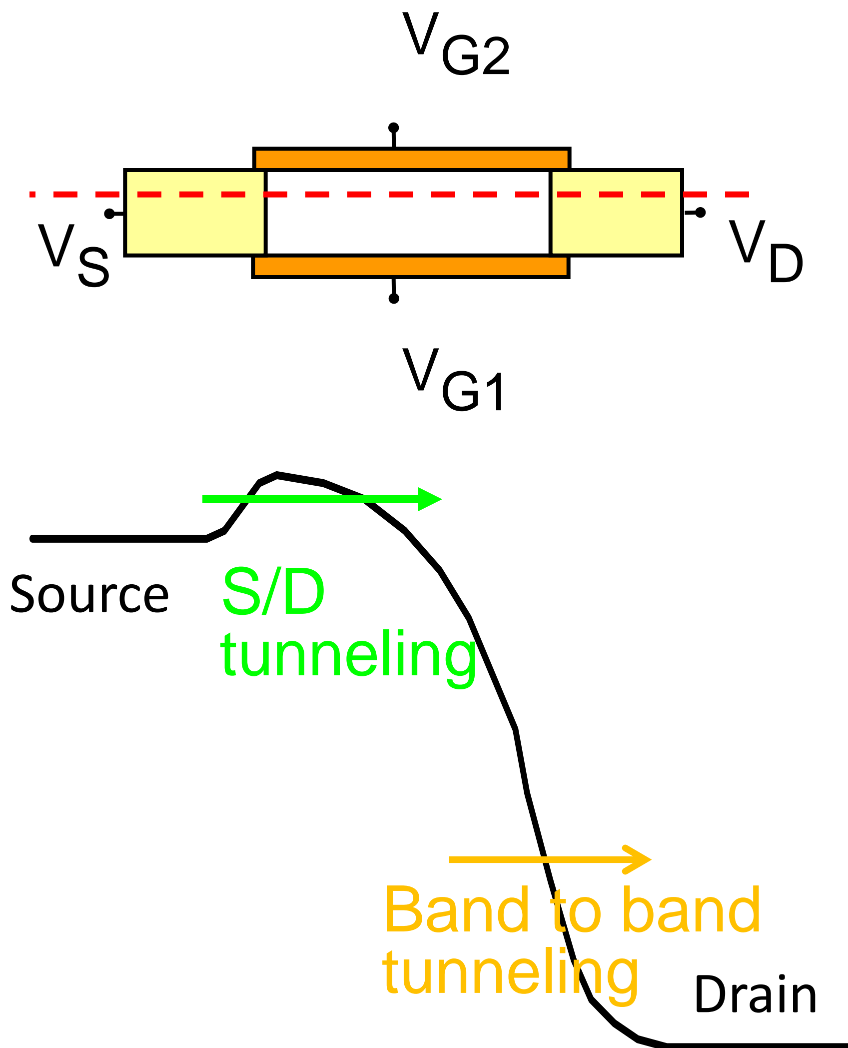
Quasi-Ballistic

$$I_{DS} = W C_g^{eff} (V_{DD} - V_T) \left[\frac{1-r}{1+r}\right] v_{inj}$$

Quantum transport effects

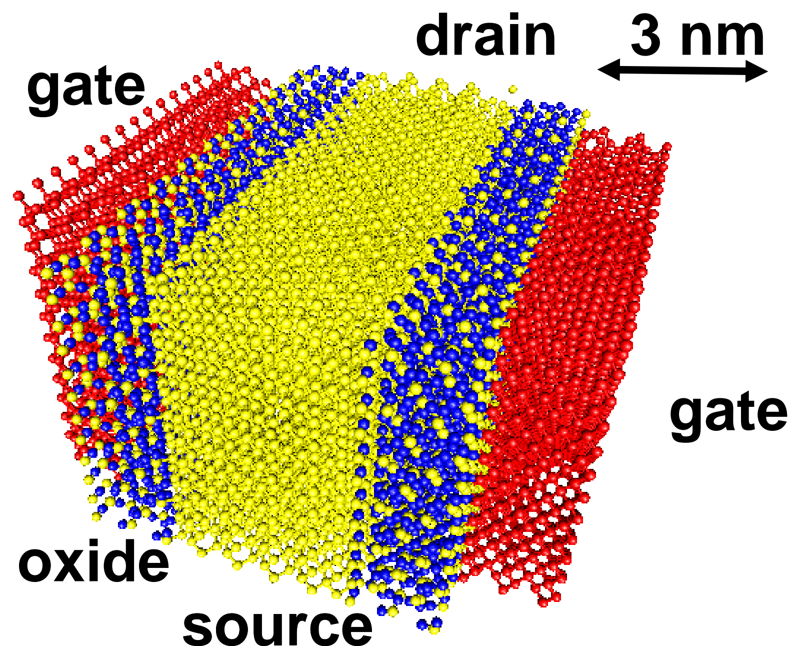


Emerging Non-Equilibrium Green's Function method to solve quantum transport in realistic device structures



Atomistic effects

- Exploit "atomistic" models to cross check predictions made with models in the continuum
- Introduce descriptions at the discrete charge & atomistic level
  - Discrete dopant effects and variability
  - Band structure calculations in Nanostructures



IU.NET

Progetti Europei IUNET in area More Moore

III-V-MOS
TCAD for III-V
MOSFETs

MODERN
CMOS Variability

IUNET

NANOSIL
Network

EUROSOI
SOI dev.

PULLNANO
32nm CMOS

ULIS
CMOS Tech.

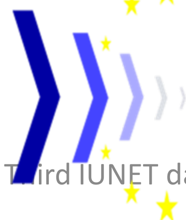
NESTOR
DG-SOI FETs

SINANO
Network

1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016

PULLNANO

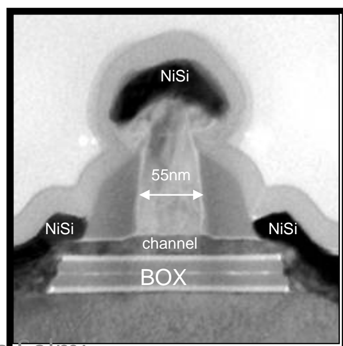
NANOSIL
Silicon-based
nanostructures
and nanodevices



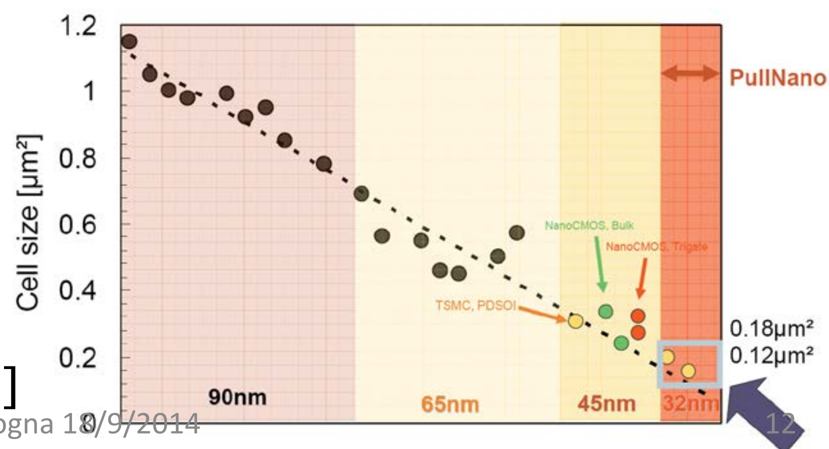
PULLNANO – PULLing the limits of NANOcmos electronics

PULLNANO

- Objective: pulling forward CMOS Technologies: demonstration of feasibility of a 32nm CMOS logic technology; exploratory action towards the 22nm node.
- Period: 06/2006 - 01/2009
- Four semiconductor companies (ST, Freescale, Philips, Infineon), Four research institutes (IMEC, CEA, Fraunhofer, CNRS), Seventeen universities/consortia, three SME; total 35 partners
- UniBO, UniUD, UniPI and PoliMI participating for IU.NET



[PULLNANO K.o.M.]



NANOSIL NoE

Objective: delivery of significant outputs in the following areas

- *WP1 – More Moore*
  - FSP 1.1 – Appraisal of new channel materials for end of CMOS era
  - FSP 1.2 – Routes to realisation of Schottky barrier contacts for end of CMOS era
  - FSP 1.3 – Identification and appraisal of gate stack materials/combinations for end of CMOS era
- *WP2 – Beyond CMOS*
- *WP3 – Joint Fabrication and processing pltform*
- *WP4 – Joint Modeling and Characterization platform*
- *WP5 – Spreading of excellence*

Period: January 2008 – Dec. 2010

IUNET partners involved: UniBO, UniUD, UniPI, PoliMi, 28 partners total

IUNET activities in PULLNANO and NANOSIL

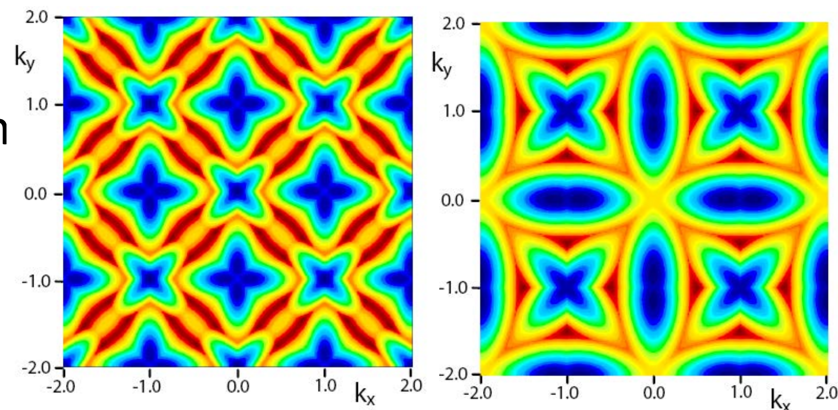
- Conduction and valence band structure calculation methods for 2D carrier gas (LCBB, KP, TB, EMA)
- Semiclassical transport models (PDE, D-BTE, MSMC)
- Quantum transport models based on NEGF
- Analytical mobility and backscattering models
- Physical effects:
  - Stress/Strain effects on electrostatics and transport
  - HK/MG related scattering mechanisms
  - Gate leakage currents and trap assisted currents
- Applications to:
  - Mobility (low field)
  - Quasi Ballistic Transport (high field)
  - Variability

In planar, FinFET and nanowire device architectures

Band structure calculations

– Linear Combination of Bulk Bands (LCBB)

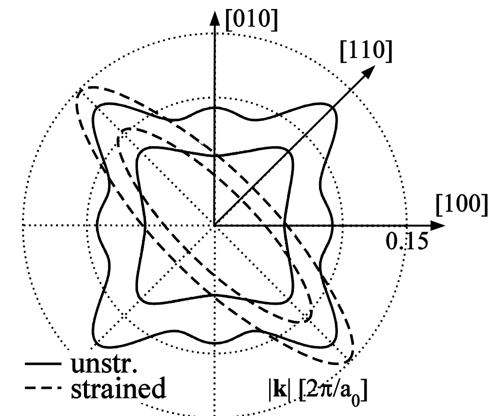
Bulk and Inv. layer, T_{Si}=5nm



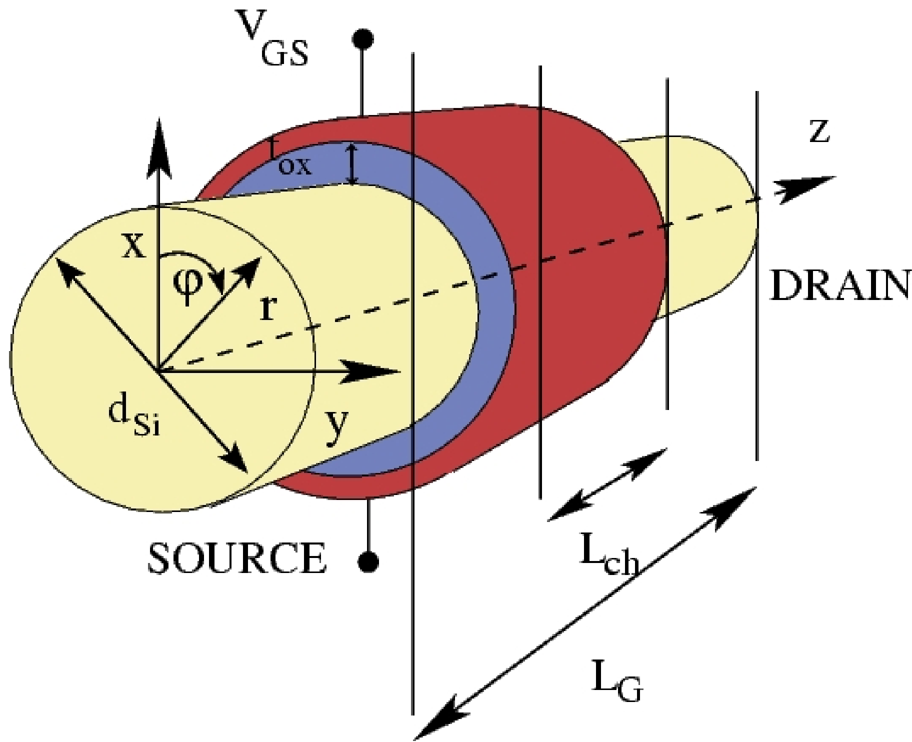
– Quantized K.P

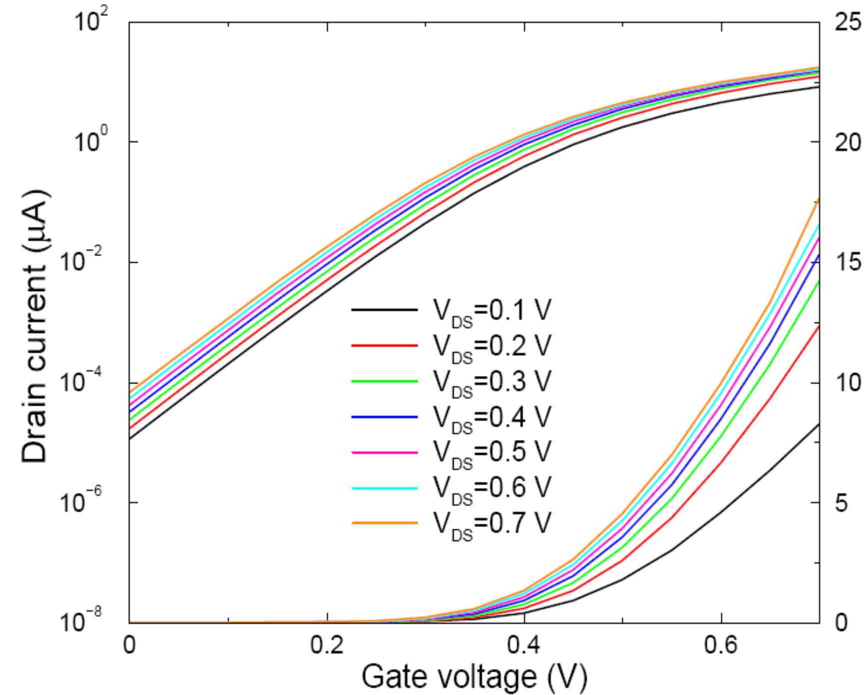
– Tight Binding

– Analytical EMA models



NEGF Quantum transport (UNIBO)



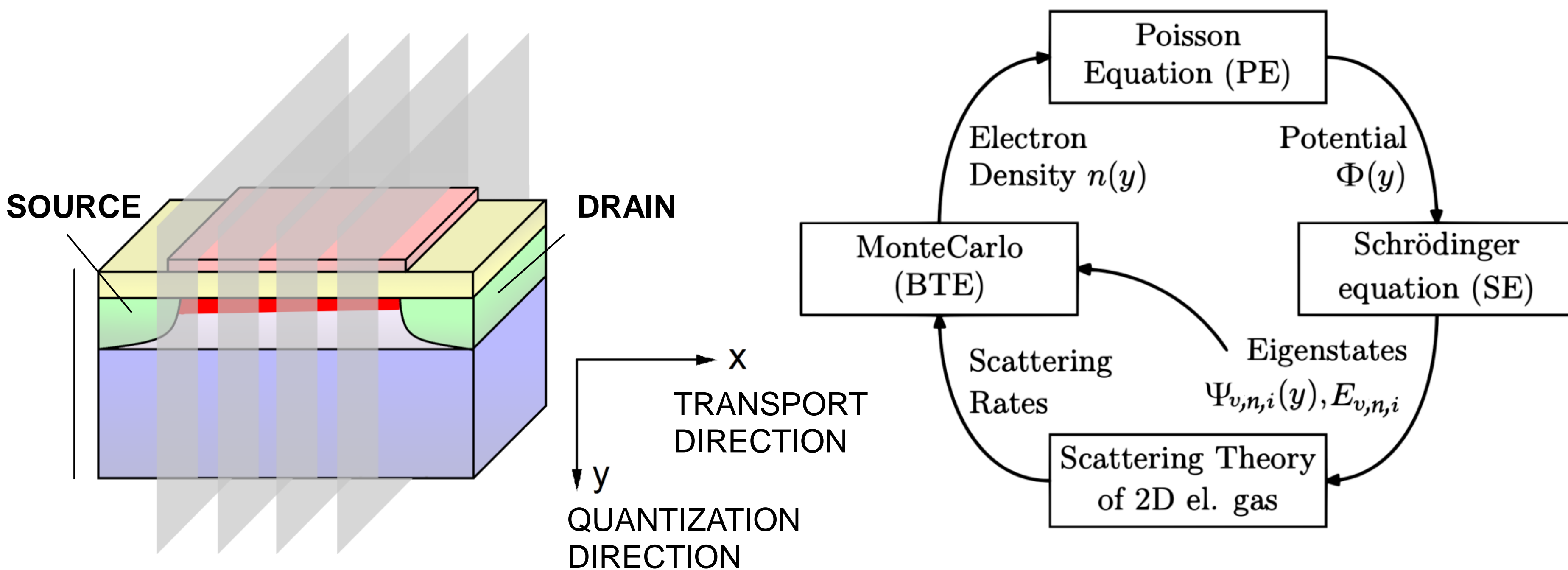


Idealized nanowire structure based on the ITRS indications for the HP 16 nm technology node

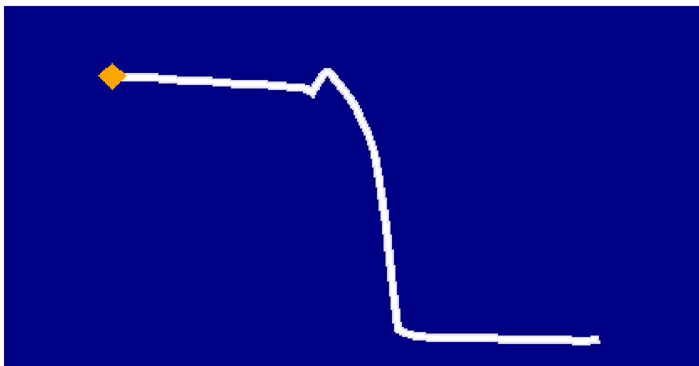
Turn-on characteristics simulated using a full-quantum model based on the open-boundary Schroedinger equation

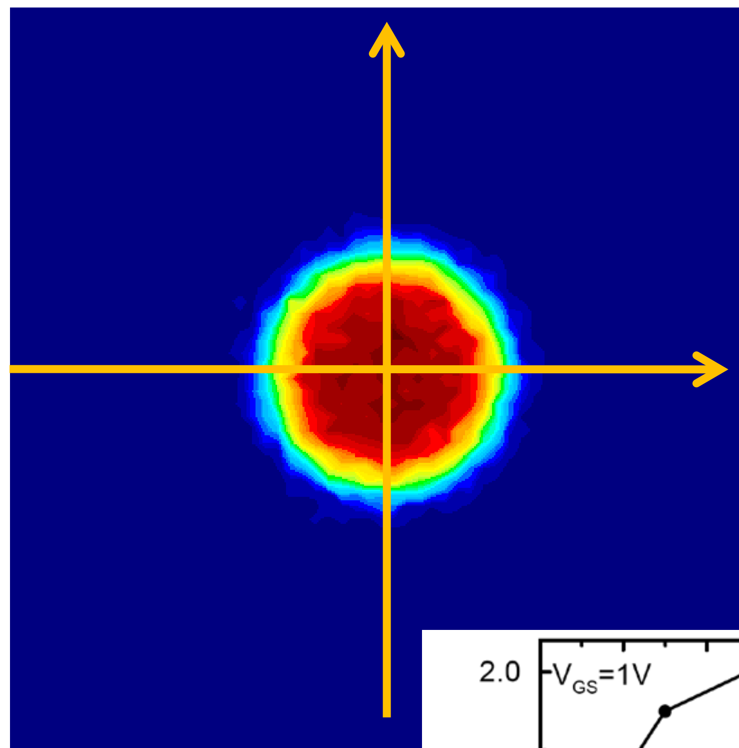
Transport models: BTE solver Multi-Subband Monte Carlo method

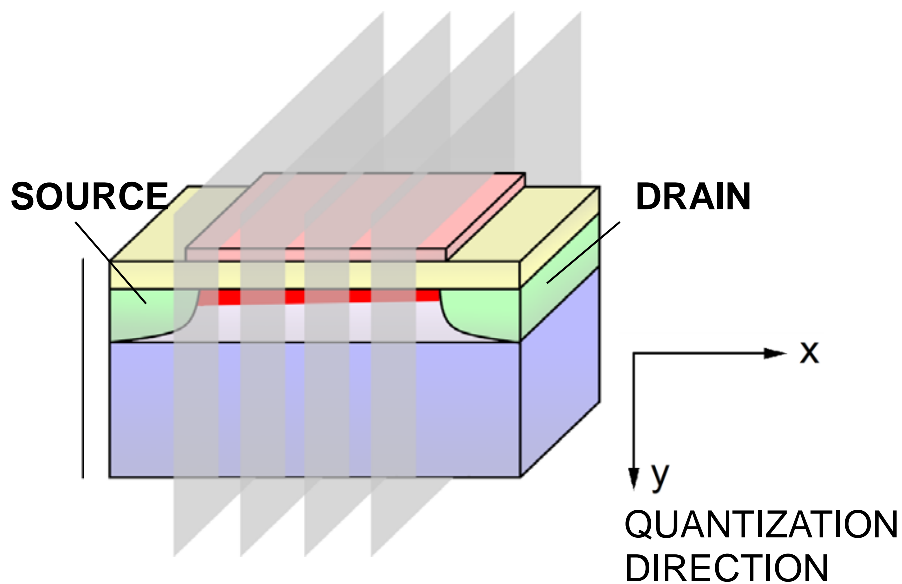
- Calculate I_{DS} characteristics of devices
- Account for vertical quantization effects
- Semiclassical description of lateral transport

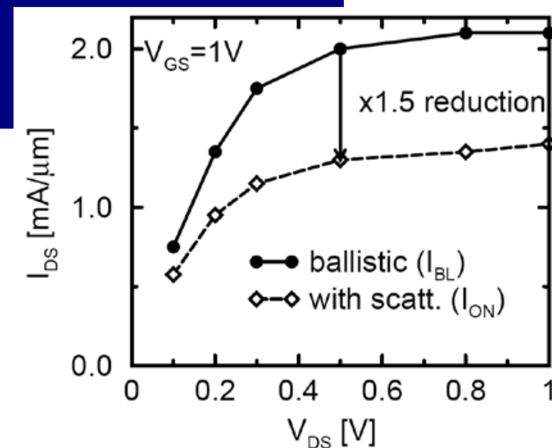


Quasi-ballistic transport

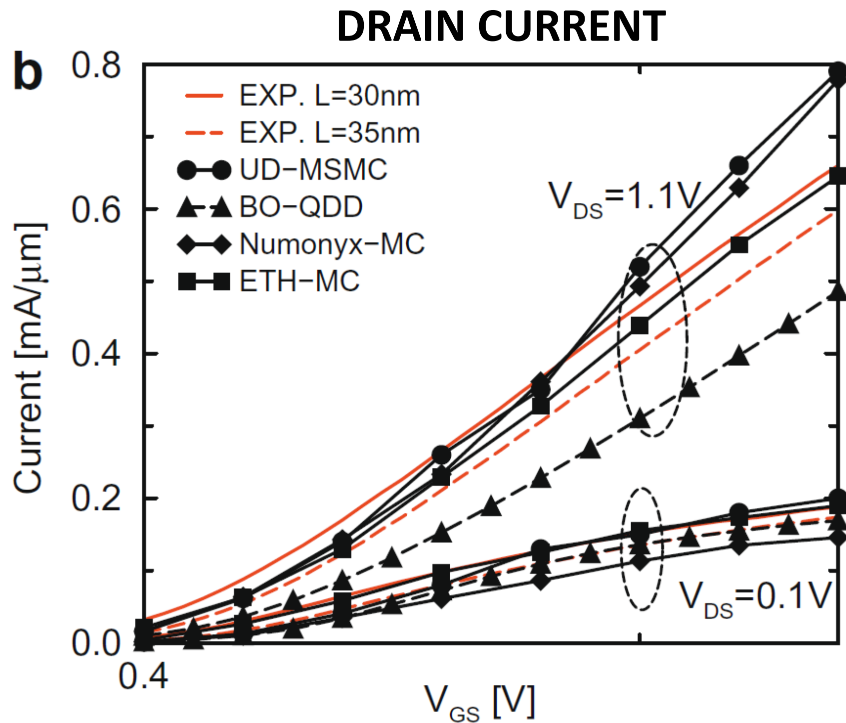


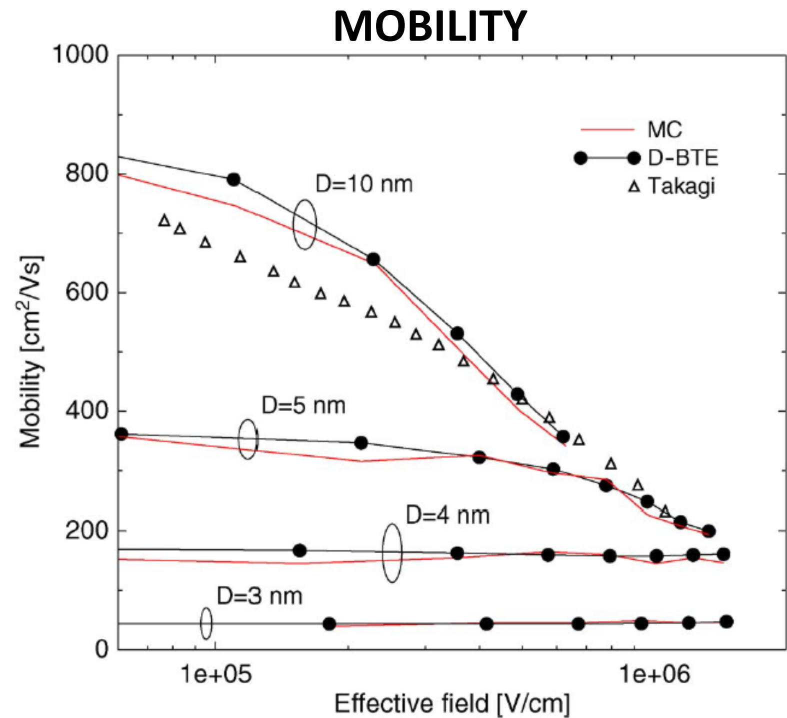






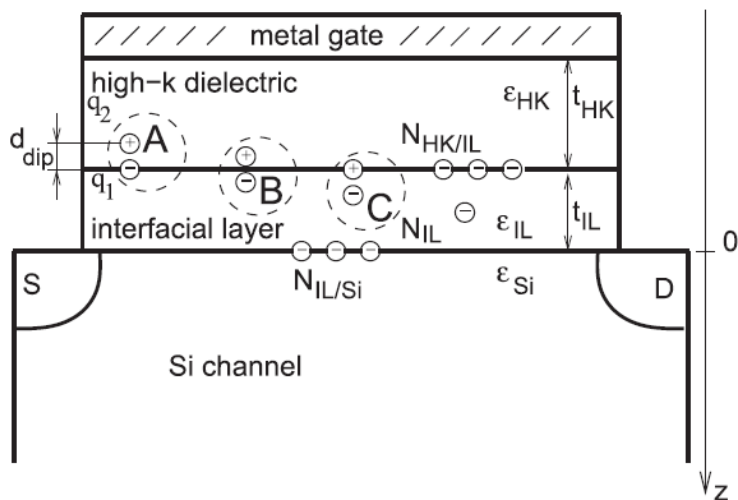
Model benchmarking: a strategy for verification

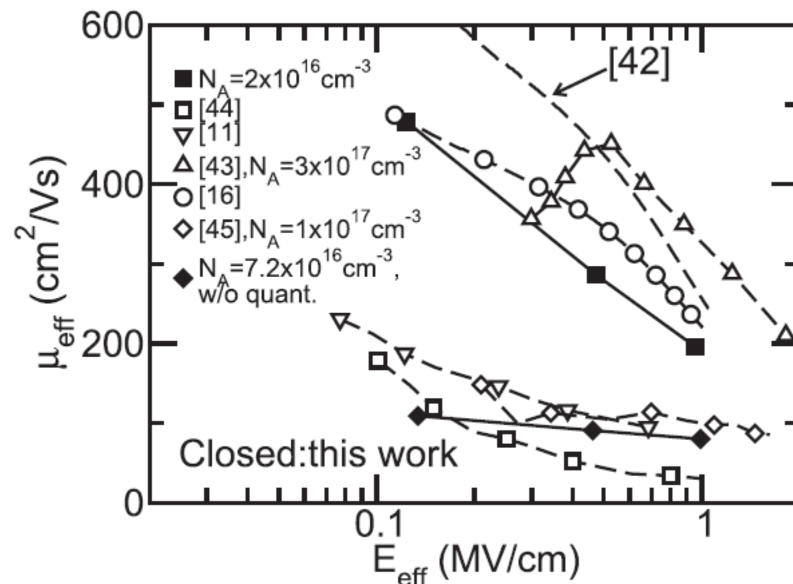




Benchmarking drain current calculations in short MOSFETs and mobility in nanowires

Mobility in HK/MG stacks



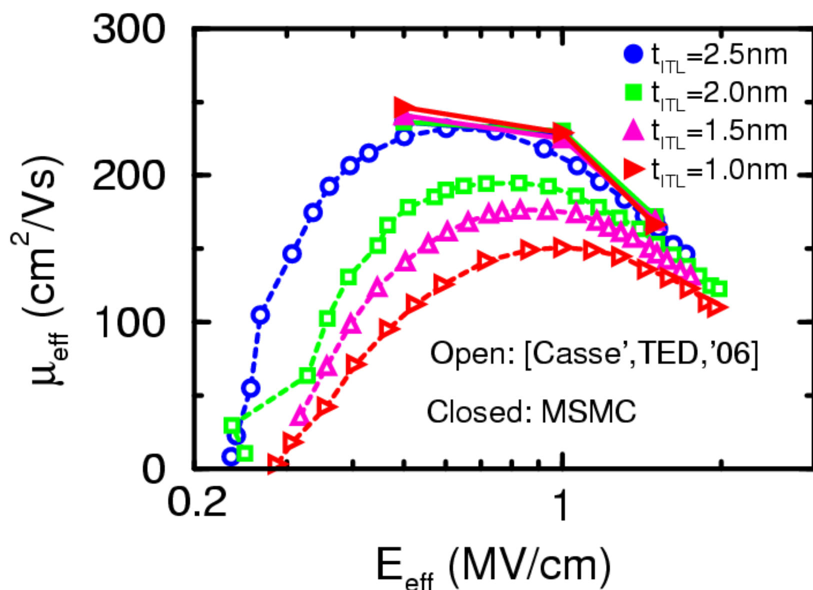


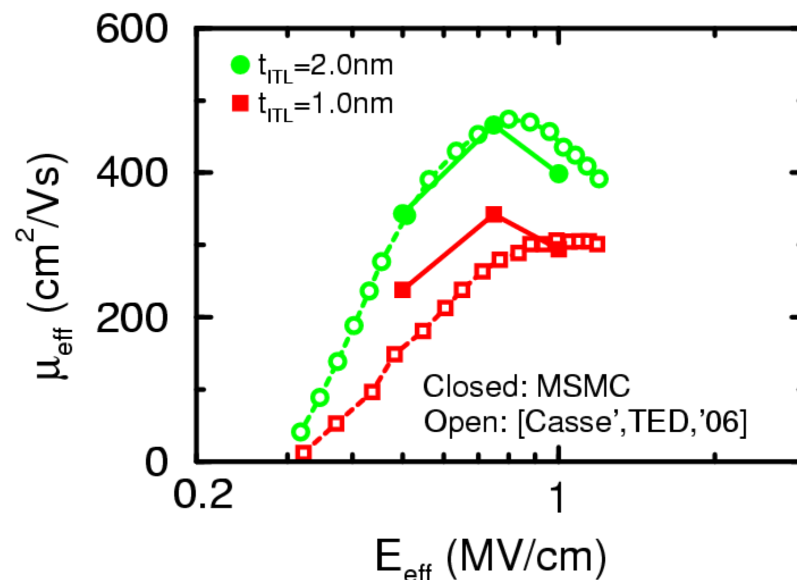
Remote phonons and remote Coulomb scattering mechanisms as possible root cause of mobility degradation in HK/MG stacks

Many possible arrangements of the charge

Extensive comparison with data from research labs and industry (IBM, ST, CEA-LETI, Tyndall)

Mobility in HK/MG stacks



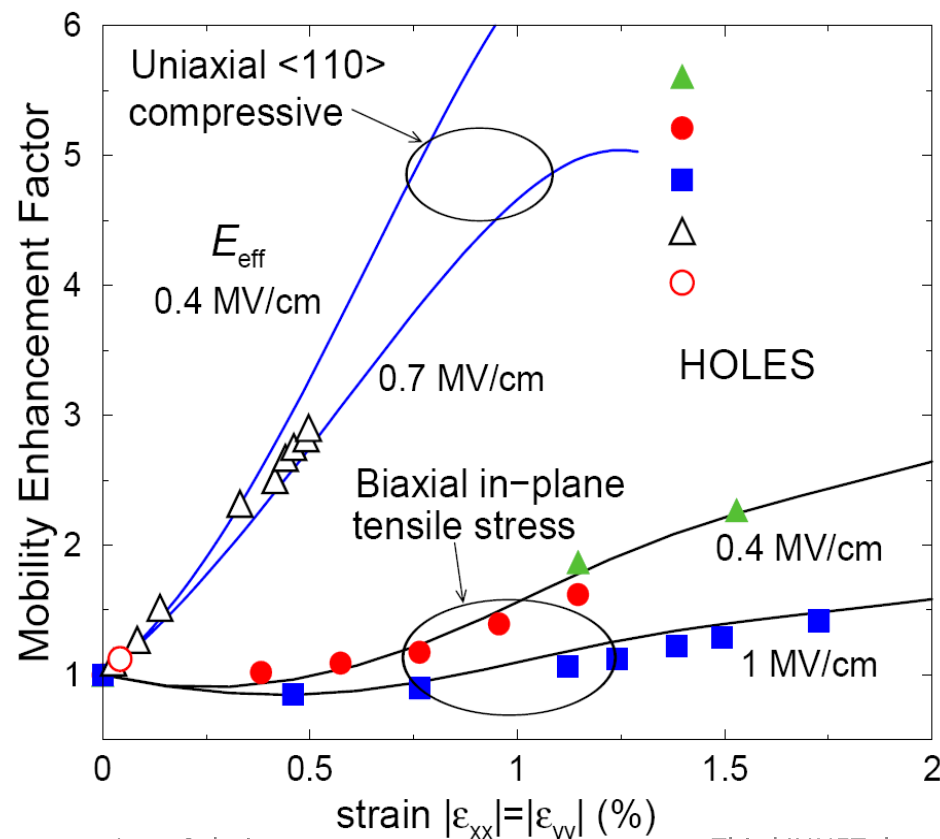


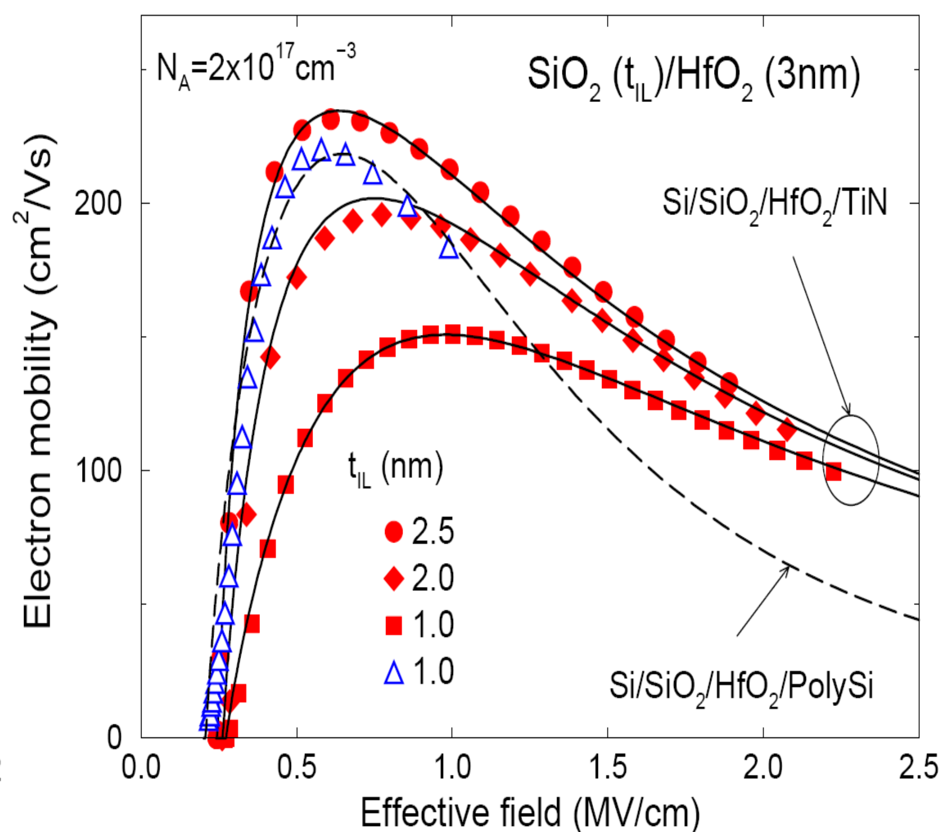
- Mobility reduction strongly mitigated by the ITL
- SOph + SR + ph limited mobility is still much higher than experimental mobility
- The mobility reduction can be explained by remote charges at the ITL/HK interface.
- Very large charge density → Vt shift not consistent with exp.

Analytical Mobility Models: IUNET-BO

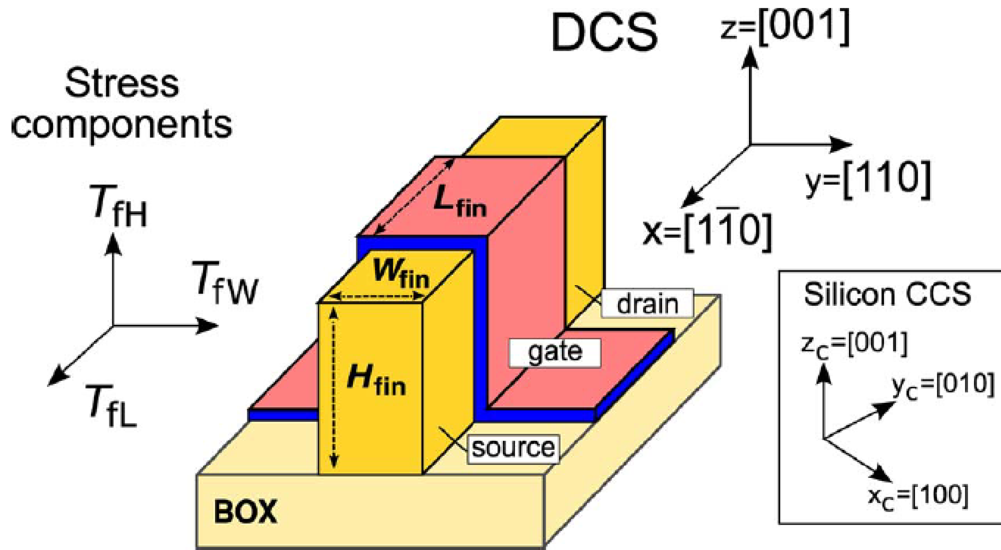
- Analytical mobility models for PDE based simulators (TCAD)

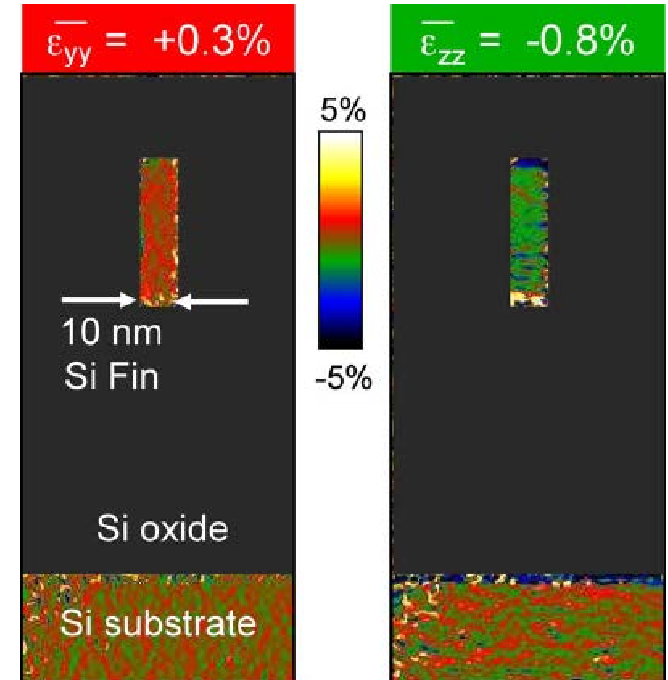
Electron and hole mobility for strained silicon and high-k stacks, ultra-thin body and different substrate/channel orientations





Stress/Strain in FinFETs

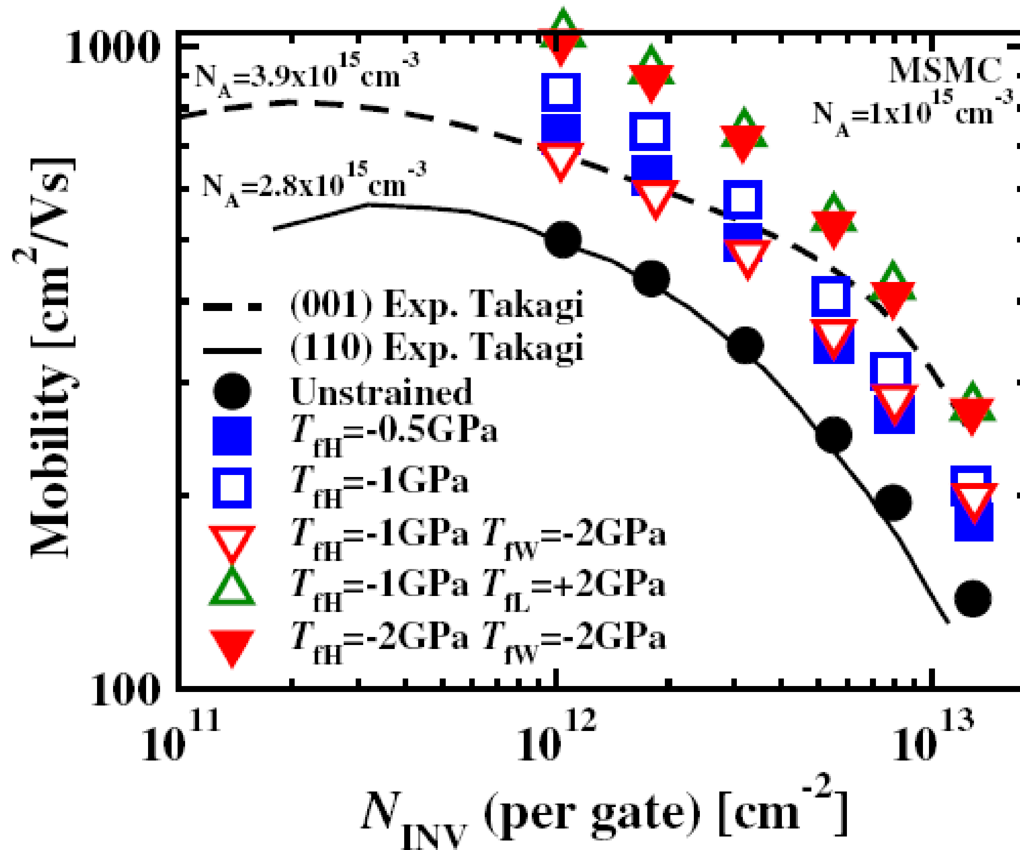




[Collaboration with NXP / Univ. Warwick]

Stress/Strain in FinFETs

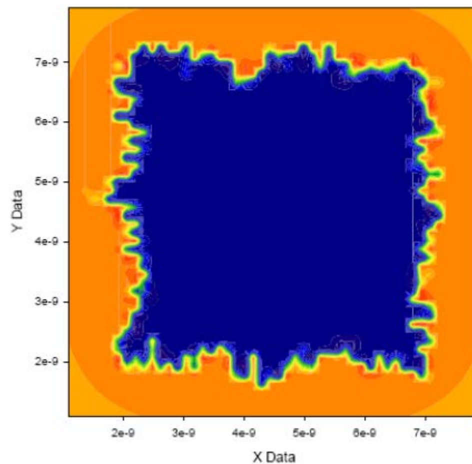
- Mobility of ***stressed*** (110)/[110] DG n-FinFETs

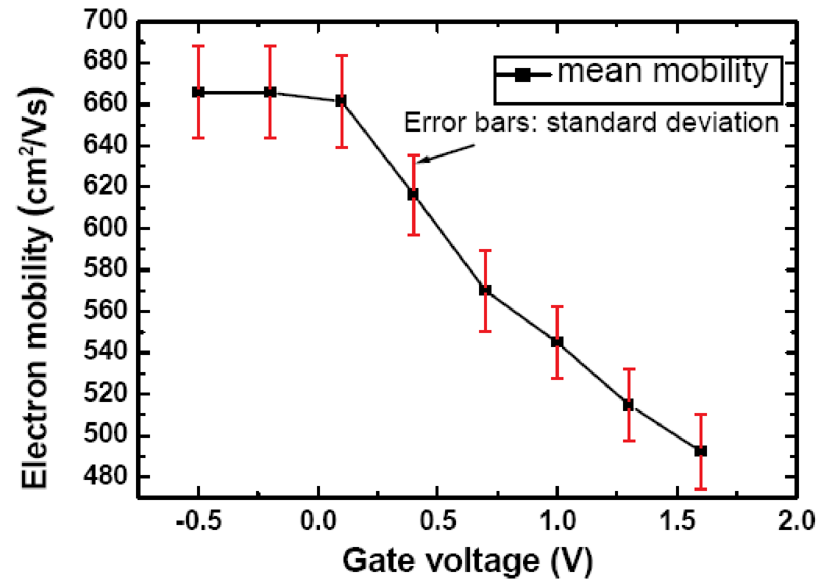


- Compressive T_{fH}
  - Δ2 re-population
- Compresive T_{fW} Tensile T_{fL}
  - Δ2 transport mass reduction (*shear strain*)

Fluctuations and Variability (IUNET-PI)

Impact of surface roughness on the mobility of planar- and wire-transistors





Methodology to derive statistical variability data from simpler sensitivity analysis and mcuh less time consuming simulations

IU.NET

Progetti Europei IUNET in area More Moore

III-V-MOS
TCAD for III-V
MOSFETs

MODERN
CMOS Variability

IUNET

NANOSIL
Network

EUROSOI
SOI dev.

PULLNANO
32nm CMOS

ULIS
CMOS Tech.

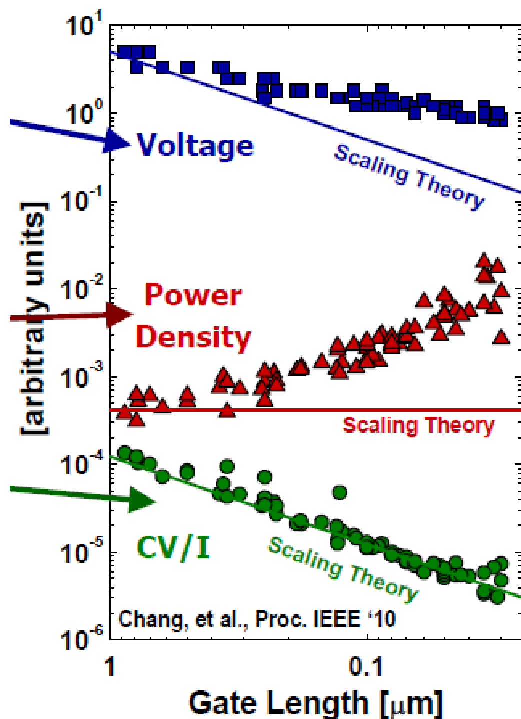
NESTOR
DG-SOI FETs

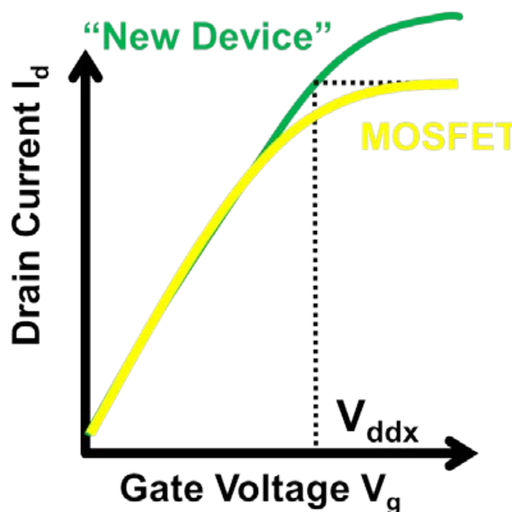
SINANO
Network

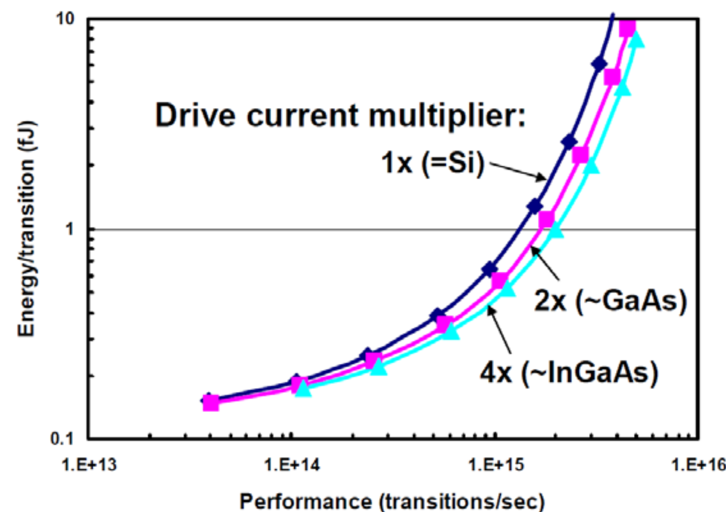
1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016

III-V-MOS Project background

- Power supply (V_{DD}) scaling is mandatory to contain power dissipation
- High mobility channels can help retain high perfomance at low V_{DD}
- After almost 10 years and 4 technology generations it is becoming increasingly difficult to keep the desired levels of strain in the channel, especially in MugFETs
- Alternative channel materials have emerged as a possible replacement for Si





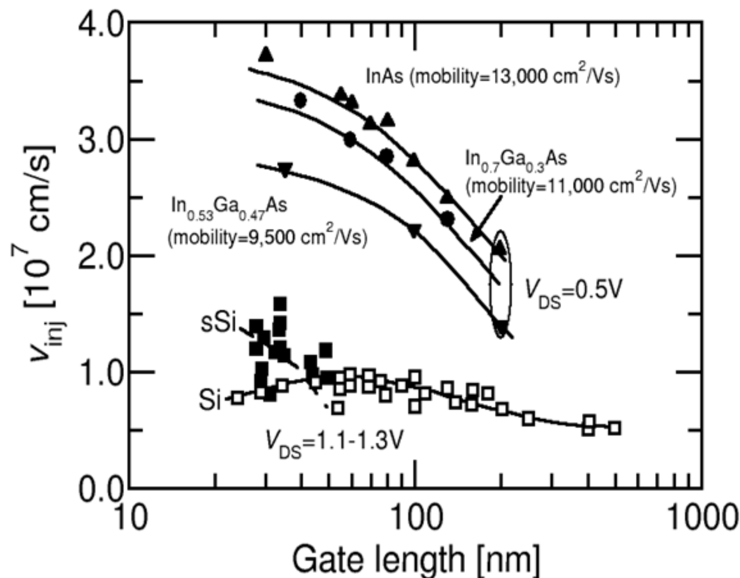


[D.Frank, SINANO Summer School 2012]

New ITRS scaling scenario and Expected ramp up of III-V technology

A new III-V/Ge MOS scenario was introduced in ITRS 2011:

	HP	LOP	LSTP	III-V/Ge
Speed (I/CV)	1	0.5	0.25	1.5
Dynamic power (CV^2)	1	0.6	1	0.6
Static power (I_{off})	1	$5x10^{-2}$	$1x10^{-4}$	1



Co-integration of InGaAs n- and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates

L. Czornomaz[1], N. Daix[1], K. Cheng[2], D. Caimi[1], C. Rossel[1], K. Lister[1], M Sousa[1] and J. Fompeyrine[1]

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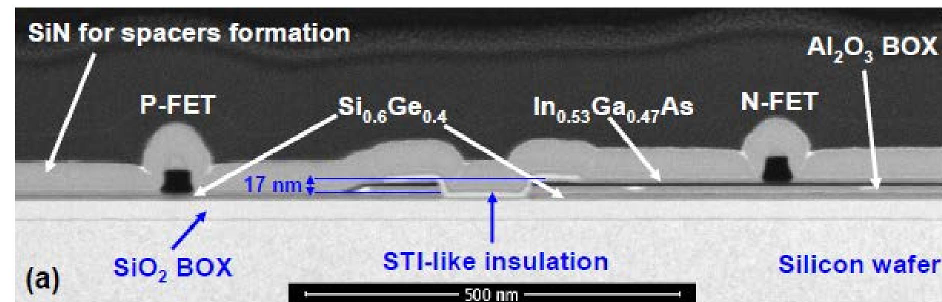
[2]IBM, 257 Fuller Rd, Albany, NY 12203, USA
Contact: luk@zurich.ibm.com



Why a III-V-MOS project now

TCAD

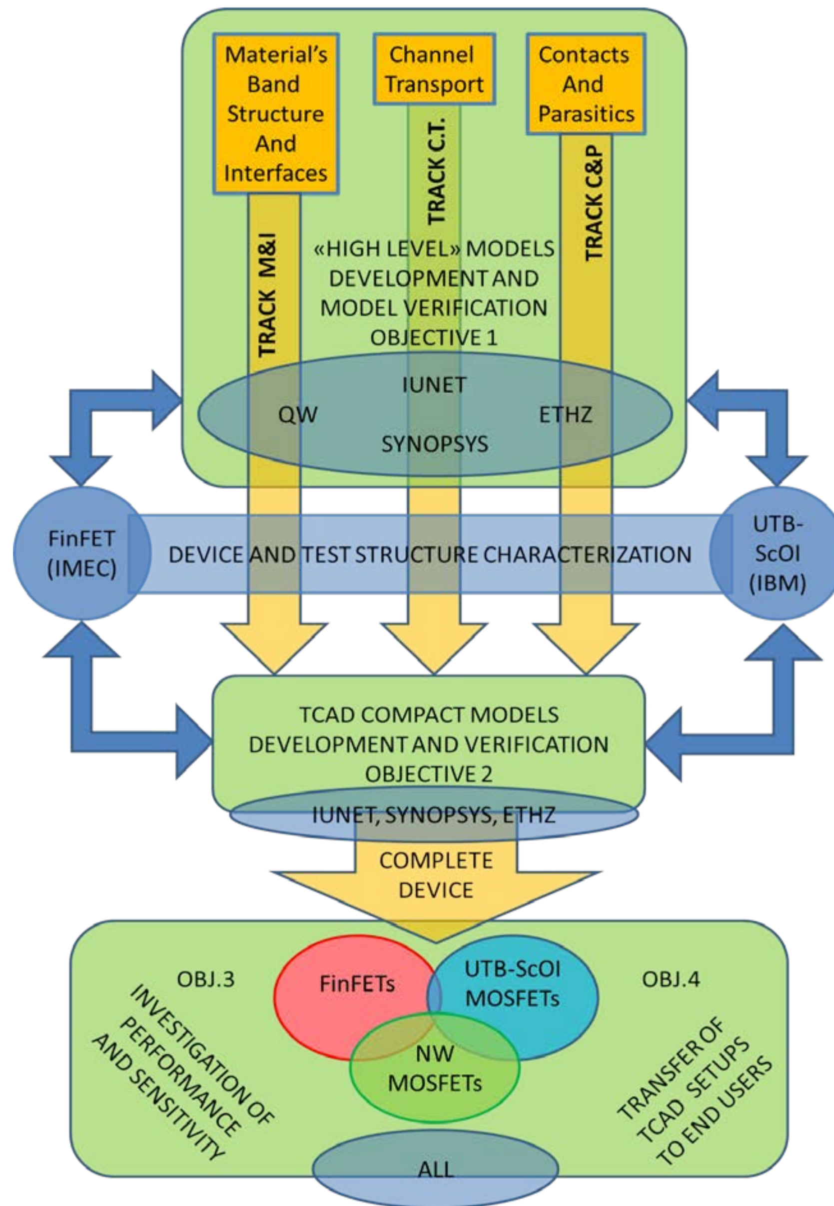
saves an estimated 40% of semiconductor technology development costs and time
enables an early assessment of new technology options also at the circuit level
assists the interpretation of experimental data and the extraction of physical parameter
is the entry point for proof of concept of new device designs

TCAD solutions should be ready well in advance of technology transfer into manufacturing
TCAD for III-V semiconductors and devices has been less developed than for Si
Semi-empirical TCAD compact models are used to extend TCAD into the nanometer scale

TCAD vendors are not in the position of offering to their customers dependable and predictive simulation tools for nanoscale III-V semiconductor n-MOS transistors

If not now, never

The project at a glance



The III-V-MOS Consortium

COMPOSITION
(# partners)

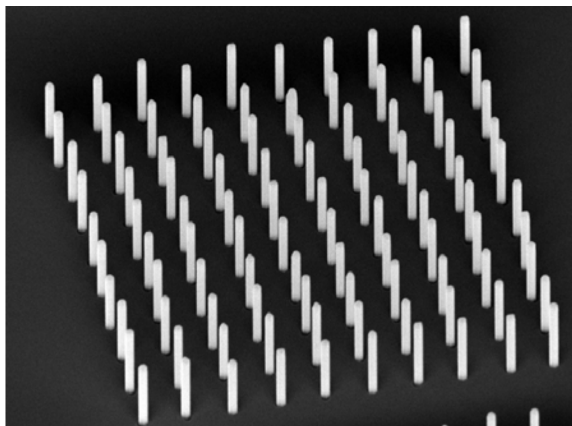
RESEARCH INST. (SI)
UNIVERSITY (IUNET, ETHZ)
SME(QW)
INDUSTRY (SNPS-CH, IBM, GF)
RESEARCH CENTER (IMEC)

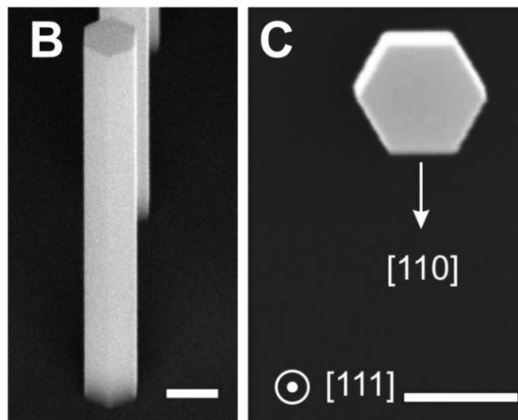
- IUNET - UD, BO, MORE (IT)
- ETH – Zurich (CH)
- IMEC (BE)
- IBM – Zurich (CH)
- QuantumWise (DK)
- GLOBALFOUNDRIES (D)
- Synopsys (CH)
- SINANO Institute (FR)

Technology and Experimental data

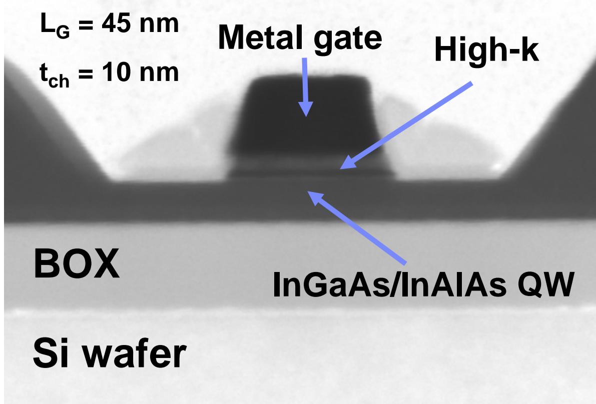
IBM

VERTICAL: Nanowire





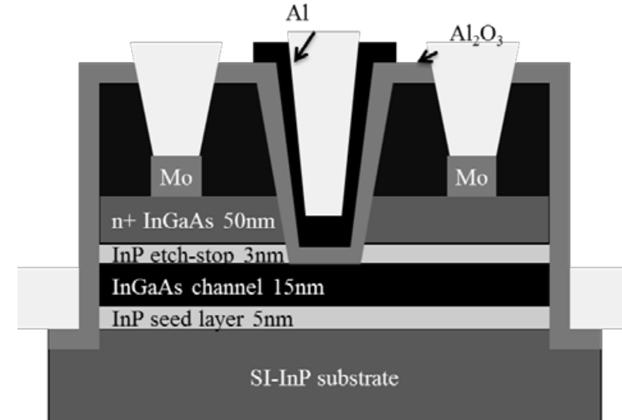
PLANAR: Wafer bonding



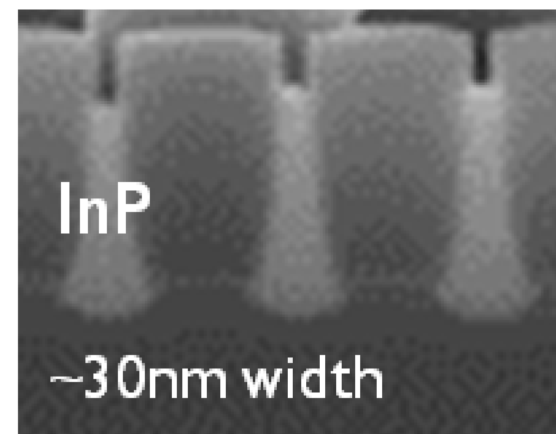
DoE for UTB InGaAs transport properties (ToF mobility and diffusivity, n+/n/n+ devices)

IMEC

PLANAR



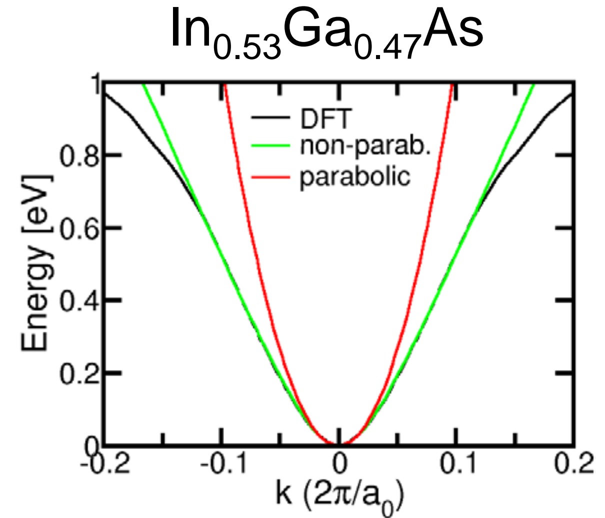
InP/InGaAs FinFET



Modeling III-V semiconductors

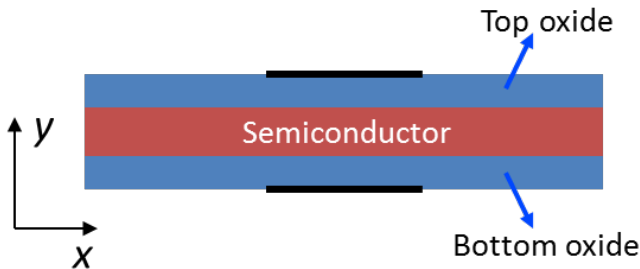
- EMA (Γ, X, L valleys) calibrated on k.p, DFT, TB, arbitrary transport and quantization directions;
- non parabolic corrections
- most relevant scattering mechanisms:
  - polar and non-polar phonons
  - remote polar phonons from the dielectric
  - surface roughness
  - local and remote coulomb scattering
  - long range coulomb

$In_{0.53}Ga_{0.47}As$



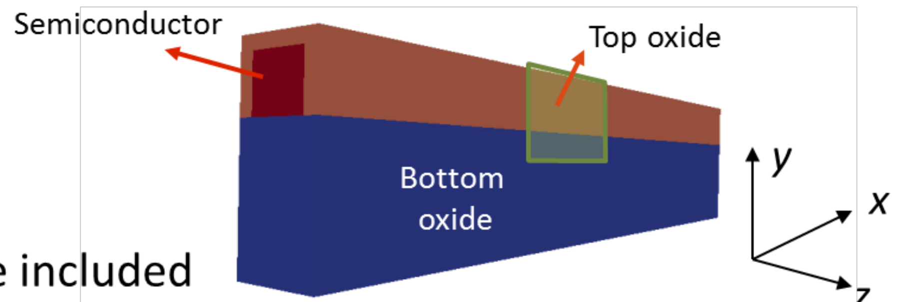
2-D structures

- UTB SOI devices



3-D structures

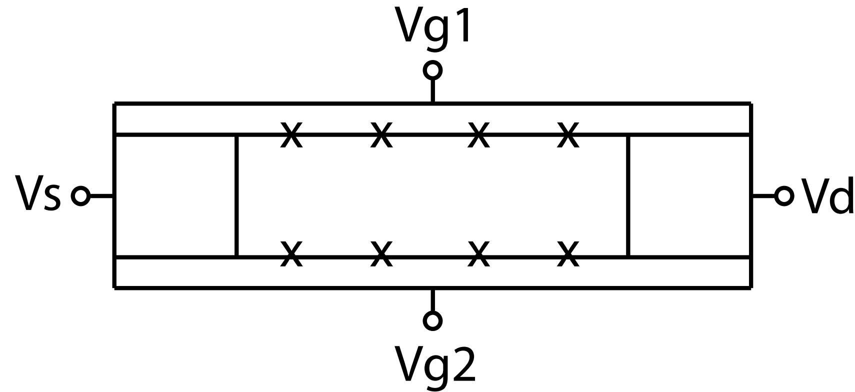
- Nanowire and FINFET-like devices

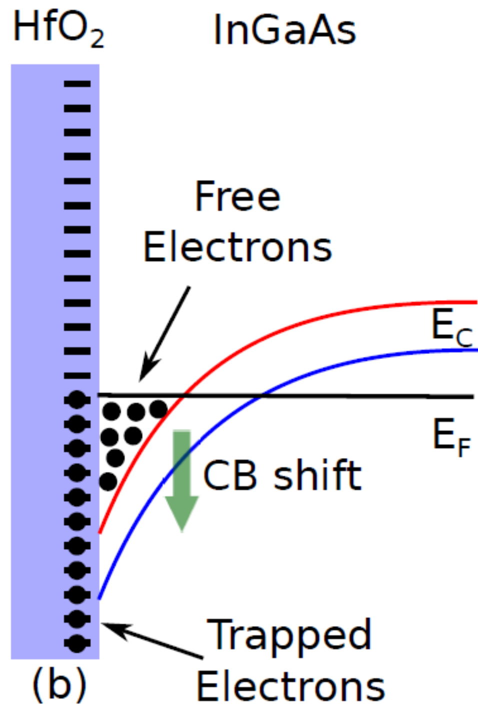


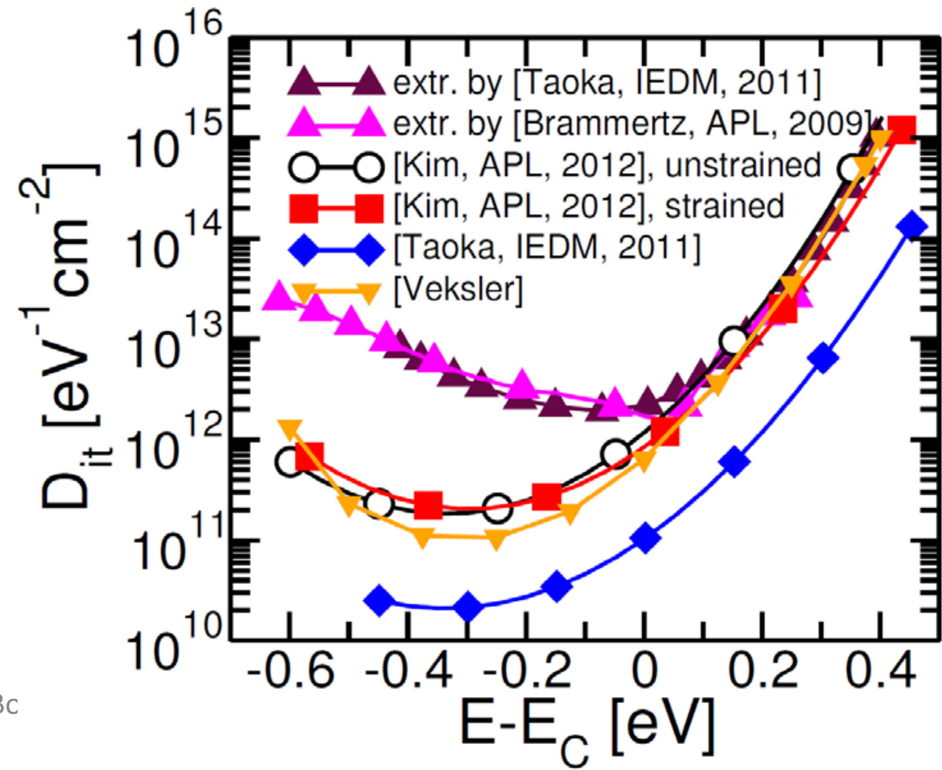
Pikus-Bir strain Hamiltonian can be included in both structures

Interface states

Electron states above midgap can capture electrons thus becoming negatively charged







Conclusioni

L'evoluzione delle tecnologie CMOS lungo la cosiddetta Legge di Moore ha fornito un contesto chiaro nel quale

- poter inquadrare le attività di ricerca
- poter reperire finanziamenti

La ricerca è stata caratterizzata da continuità e stabile crescita di competenze focalizzate

Il contenuto delle ricerche si è arricchito di indispensabili elementi di scienza dei materiali

E' prevedibile che la domanda di ricerca tecnologica finalizzata all'elettronica di basso consumo non venga meno nei prossimi anni

Il panorama internazionale è molto cambiato, la rete di relazioni deve tenerne conto

Il legame con i laboratori di fabbricazione e caratterizzazione condiziona le attività svolte

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Thank you