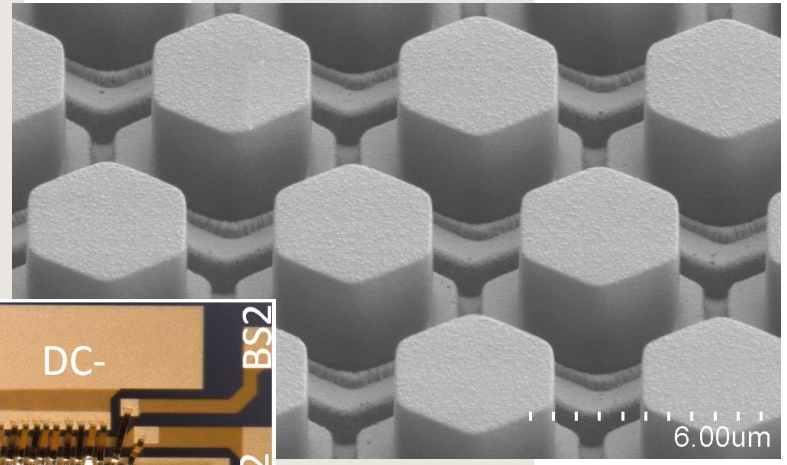
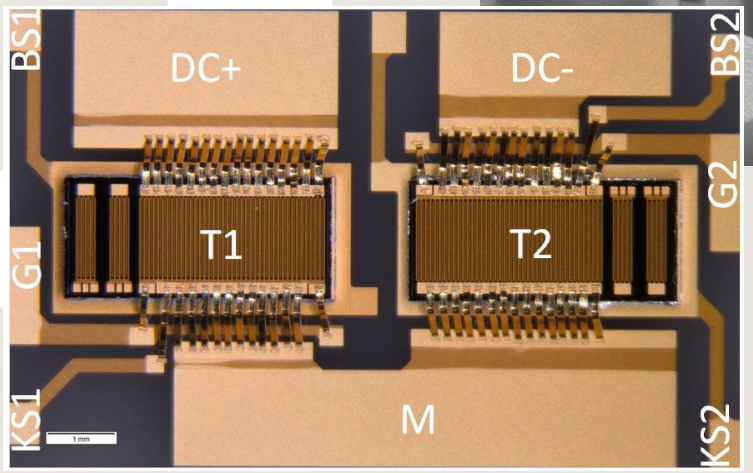
GaN and Ga_2O_3 power switching devices in lateral and vertical topology: Technologies and application possibilities

Joachim Würfl
Ferdinand-Braun-Institut
Leibniz-Institut für Höchstfrequenztechnik
Gustav-Kirchhoff-Strasse 4
12489 Berlin – Germany

Email: joachim.wuerfl@fbh-berlin.de





IUNET Workshop, September 11th, 2020

Outline

- Introduction
- Lateral devices
  - GaN, AlN, AlScN and Ga_2O_3 devices
  - Device technology
- Vertical devices
  - GaN and Ga_2O_3
- Conclusions

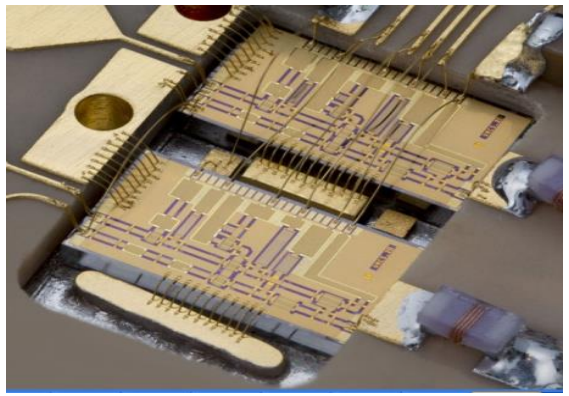
What makes Wide Bandgap Devices (WBG) attractive?

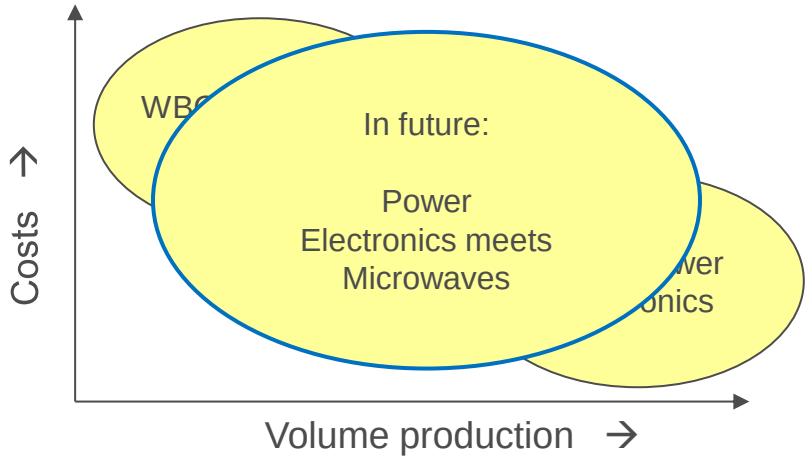
High bias voltage combined with high current density at a given geometrical dimension

→ compact, low weighted systems
→ high power levels at high frequencies
→ low internal capacitances feature fast switching

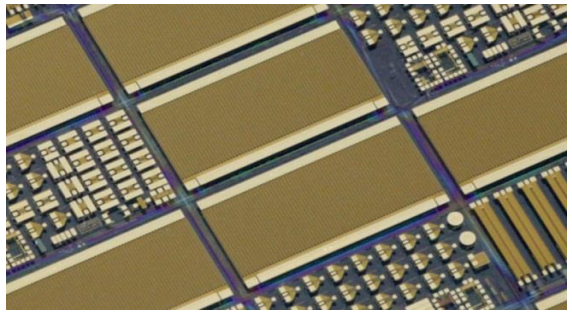
New possibilities for innovative systems
"Only works with WBG"

Microwave electronics





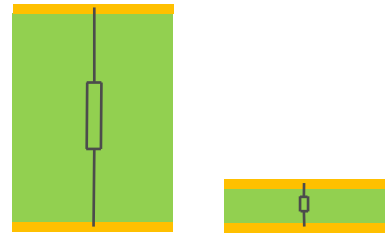
Power electronics



Comparison of device families

	Si	4H-SiC	GaN (epi)	GaN (bulk)
Band gap energy E_g (eV)	1.1 ind.	3.26 ind.	3.42 dir.	3.42 dir
Dielectric constant	11.9	10.1	9	9
Electron mobility μ_e (cm^2/Vs) *** In 2-DEG at AlGaN / GaN heterojunction**	1350	900	1150 (2000)*	1150 (>2000)*
Electric breakdown field E_{crit} (10^6 V/cm)	0.3	2.2	3.3	3.3
Saturation velocity v_{sat} (10^7 cm/s)	1.0	2.0	3	3
Thermal conductivity κ (W/Kcm)	1.5	4.9	1.3	2.3
Baliga FOM BFM$\|_{Si}$ ($\varepsilon\mu E_{crit}^3$) [1]	1	223	190 (330)*	850 (1480)*
Johnson FOM JFM$\|_{Si}$ ($v_{sat}^2 E_{crit}^2$) [2]	1	215	400	1090
Maximum estimated operation temperature T_{max} (°C)	200	500	500	500

Drift length to achieve certain breakdown voltage



Silicon GaN

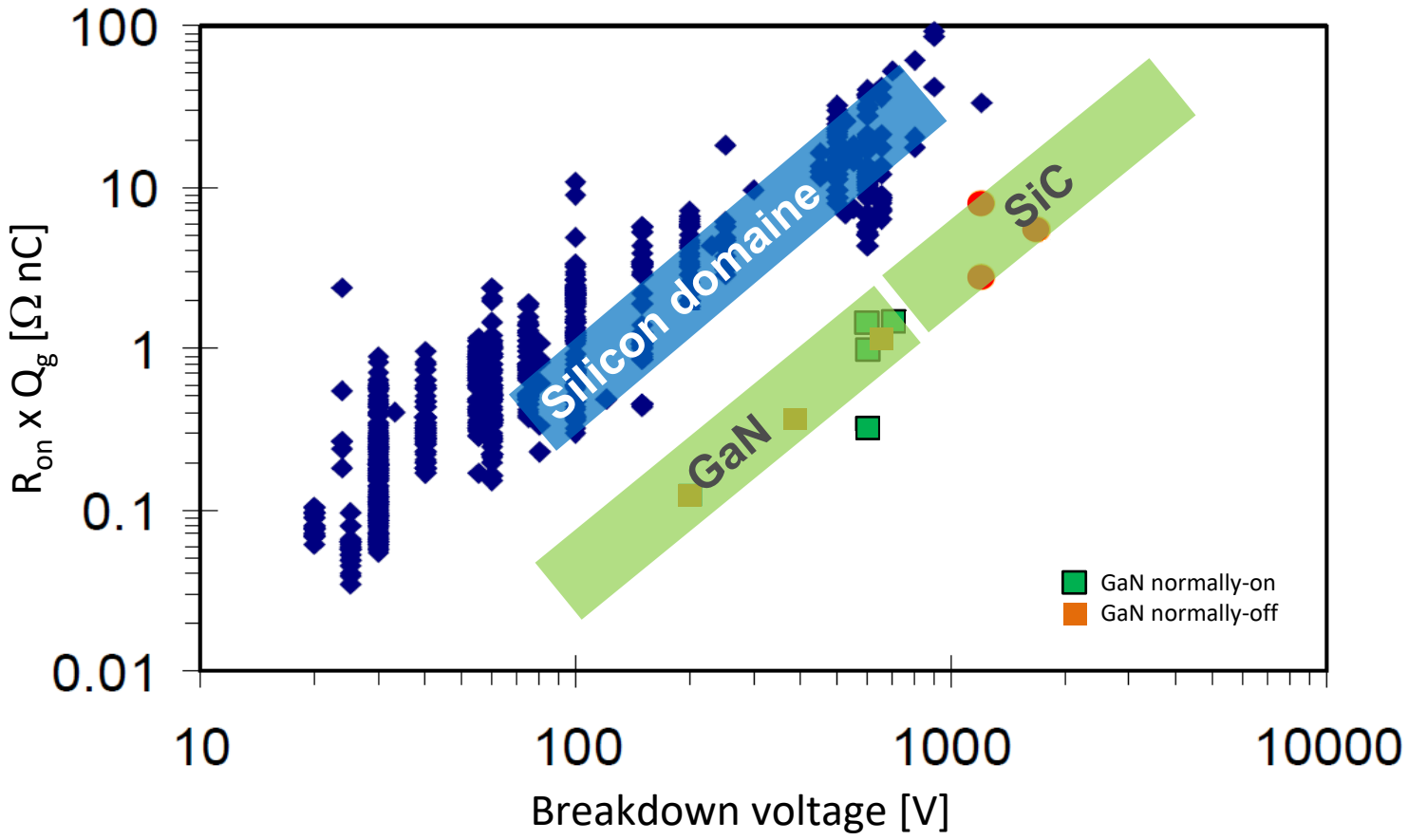
Would be motivation for vertical GaN devices

[1] B.J. Baliga, "Semiconductors for High-Voltage, Vertical Channel Field-Effect Transistors," *J.Appl.Phys.*, vol.53, no.3, pp.1759-1764, 1982

[2] Physical limitations on frequency and power parameters of transistors, RCA Review, vol. 26, pp. 163-177, June 1965.

*** In 2-DEG**

New GaN devices promise fast and efficient power switches



R_{on} x Q_g:

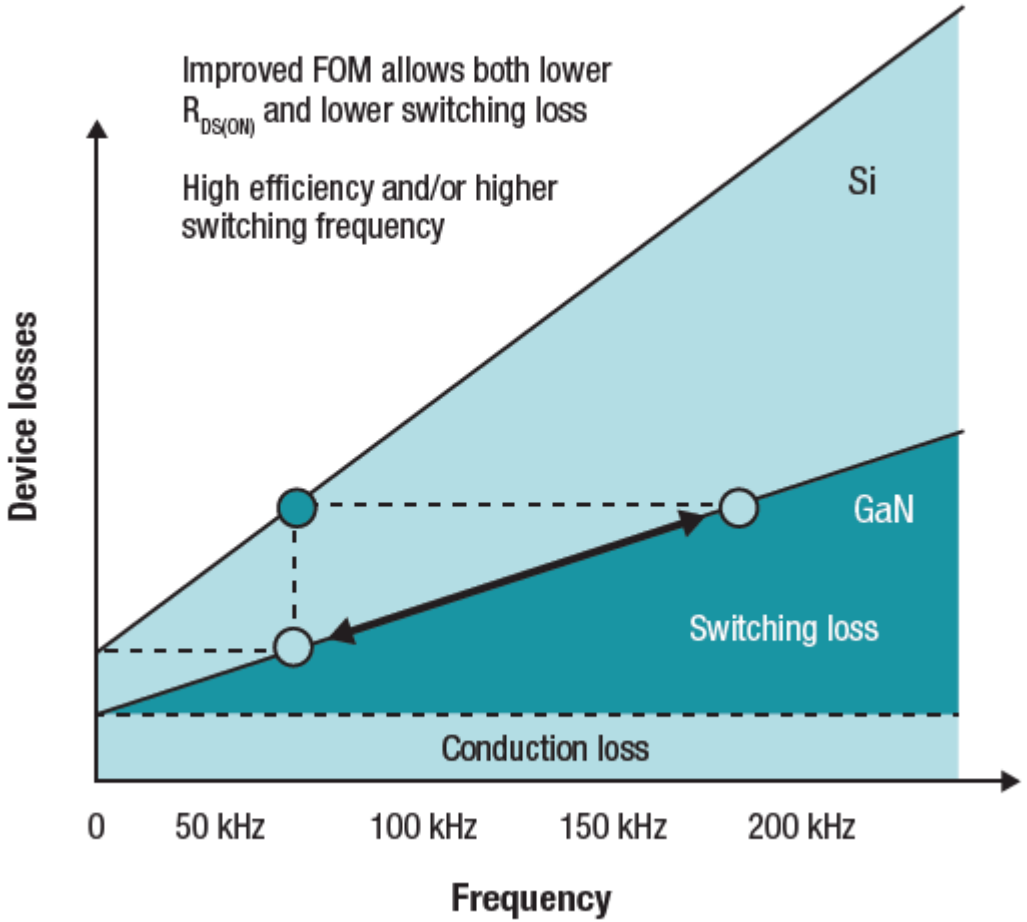
- measure for efficient switching properties

Requirements for efficient switches:

- Low dynamic on-state resistance
- Small gate charge

Leibniz Ferdinand Braun Institut

Advantages of GaN power switching devices against Si



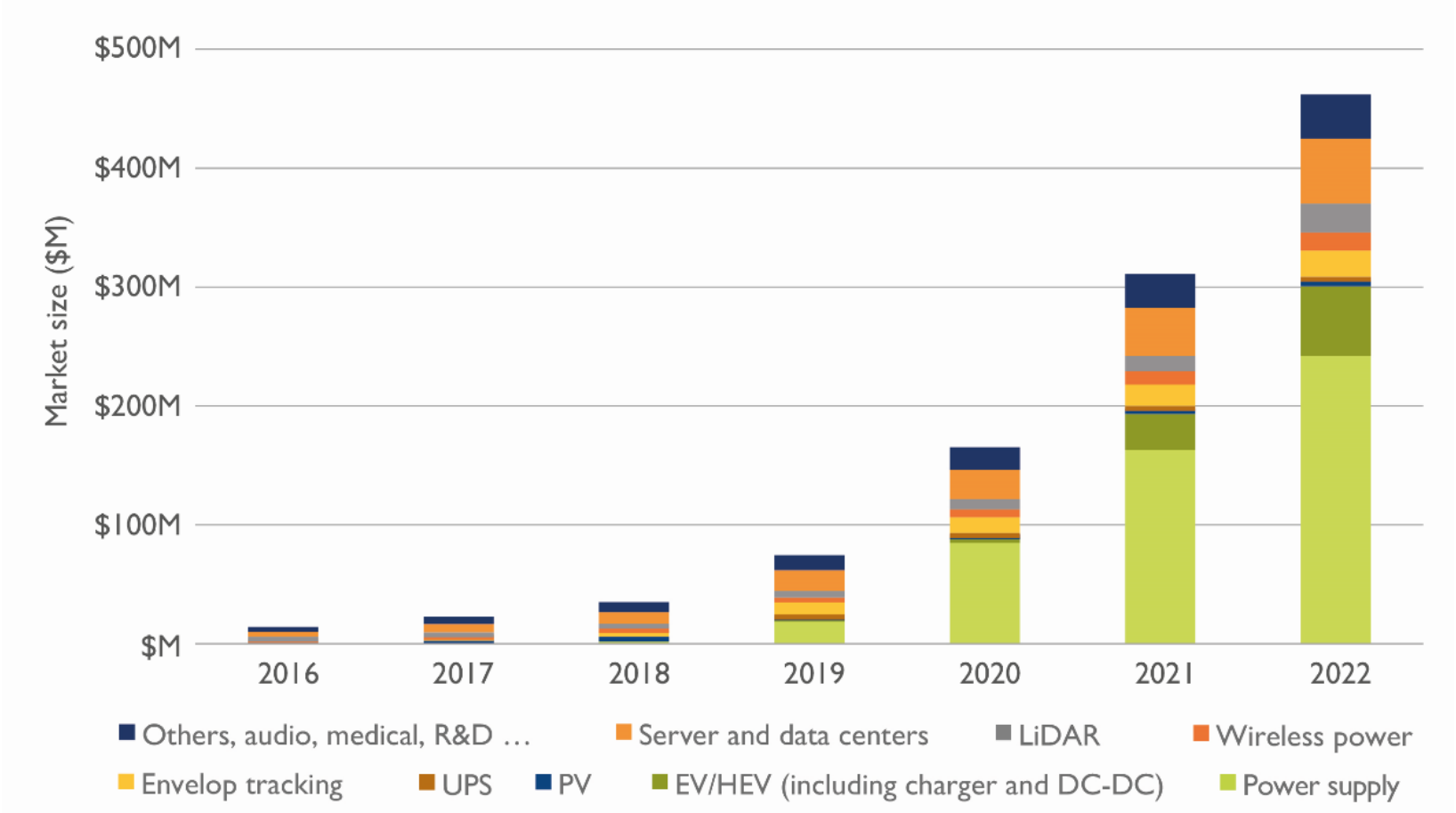
GaN efficiency advantage comes through

- Replacing Si by GaN power devices **in combination with** system level changes
- Increase slew rate and switching frequency
- Circuit topology to be optimized for GaN

Taken from Steve Tom, Texas Instruments: GaN drives energy efficiency
to the next level (https://www.electronicdesign.com/power-management/gan-drives-energy-efficiency-next-level)

Actual and potential GaN application areas (TI view)

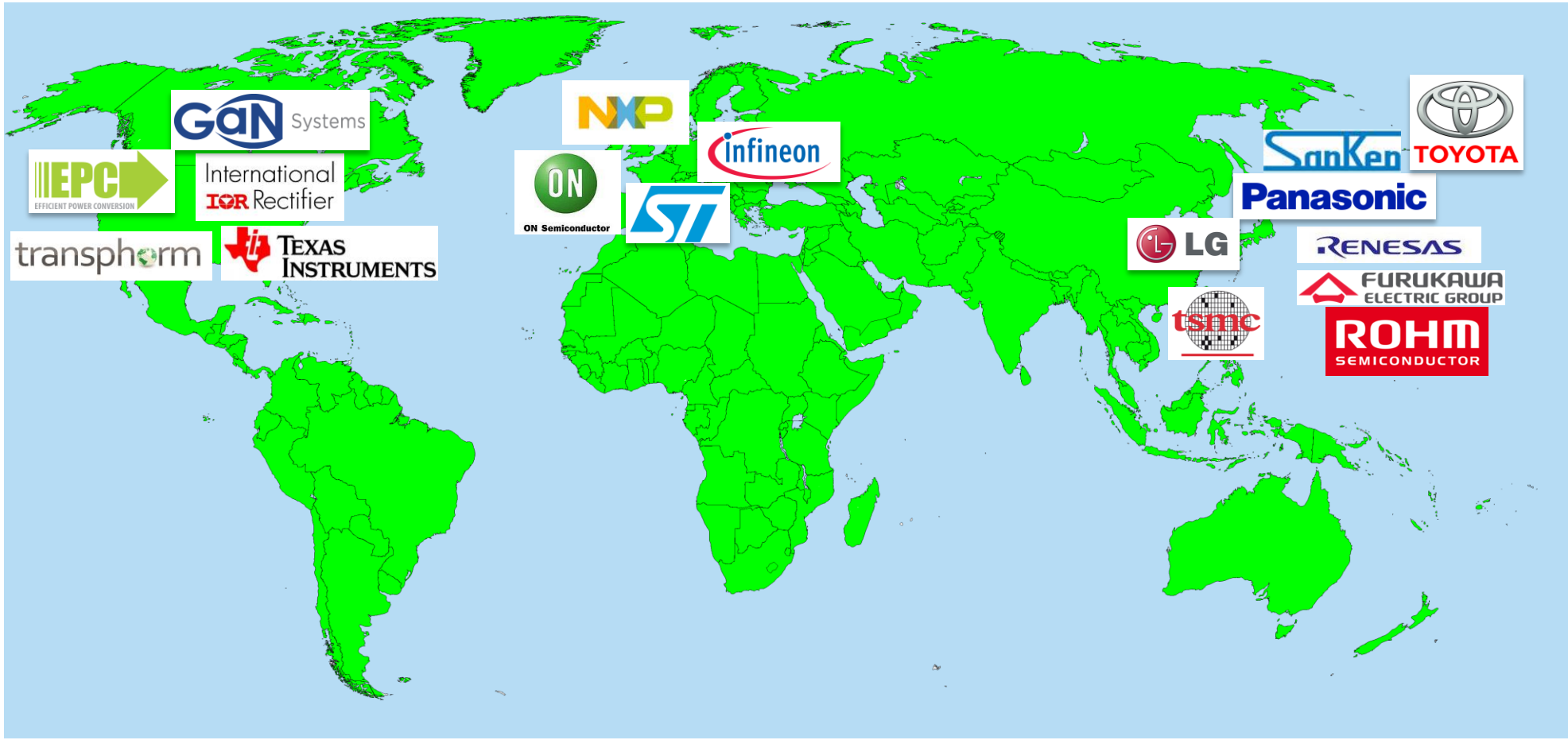
GaN power device market size split by application



Source:

Power GaN 2017: Epitaxy, devices, applications and technology trends 2017 report, Yole Developpement, October 2017

Industrial GaN power activities



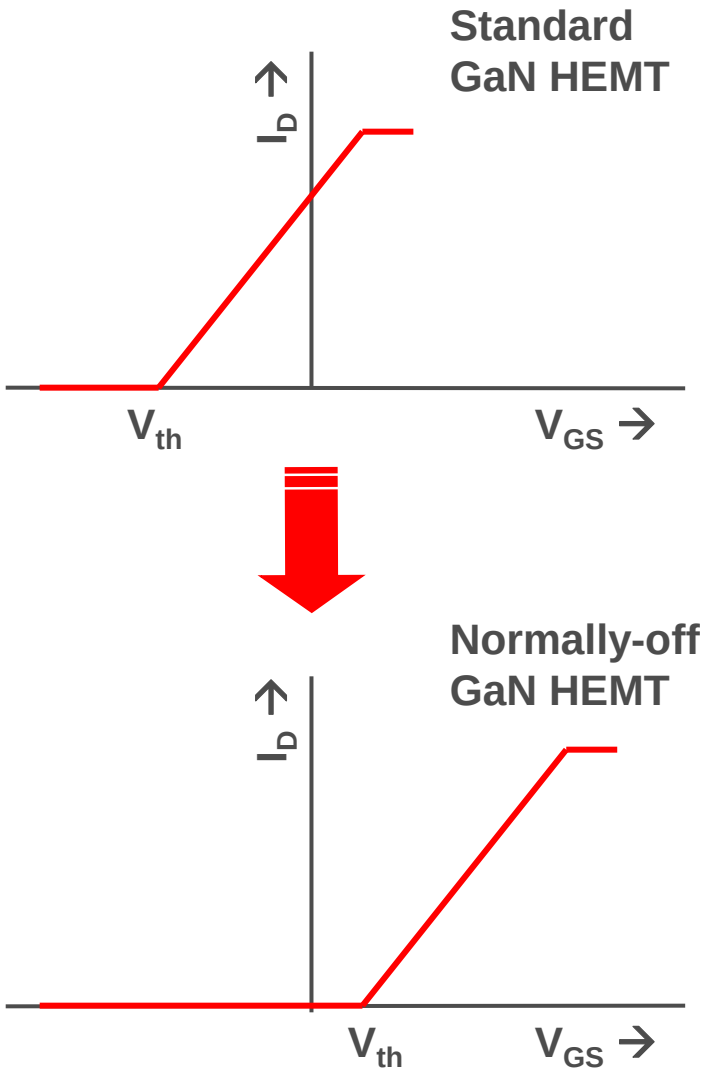
Leibniz Ferdinand Braun Institut

GaN Power electronics: General targets

- Low on-state resistance
  → outperforming other device families
- High breakdown voltage (up to 1000V)
- Threshold voltage V_{th} > +1 V
- Large gate voltage swing > 3 V
- Low leakage currents
- Reproducible process
- Reliability

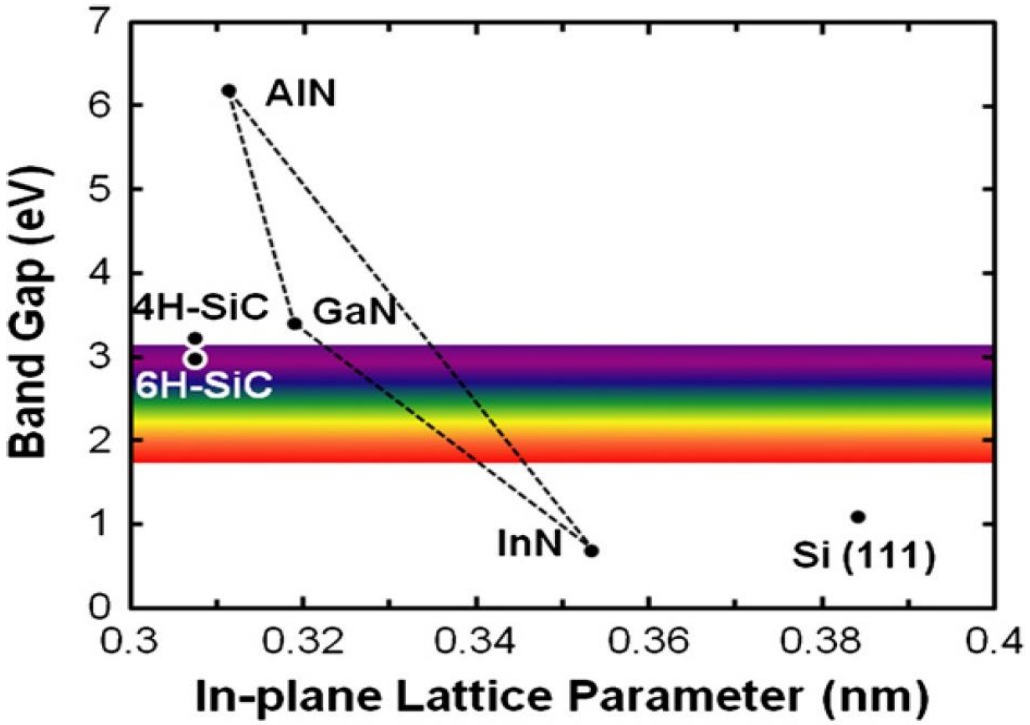
- In same cases: Radiation hardness

Most important:
Good dynamic witching properties



Substrates for GaN devices

Lattice matching of epi-layers, substrates

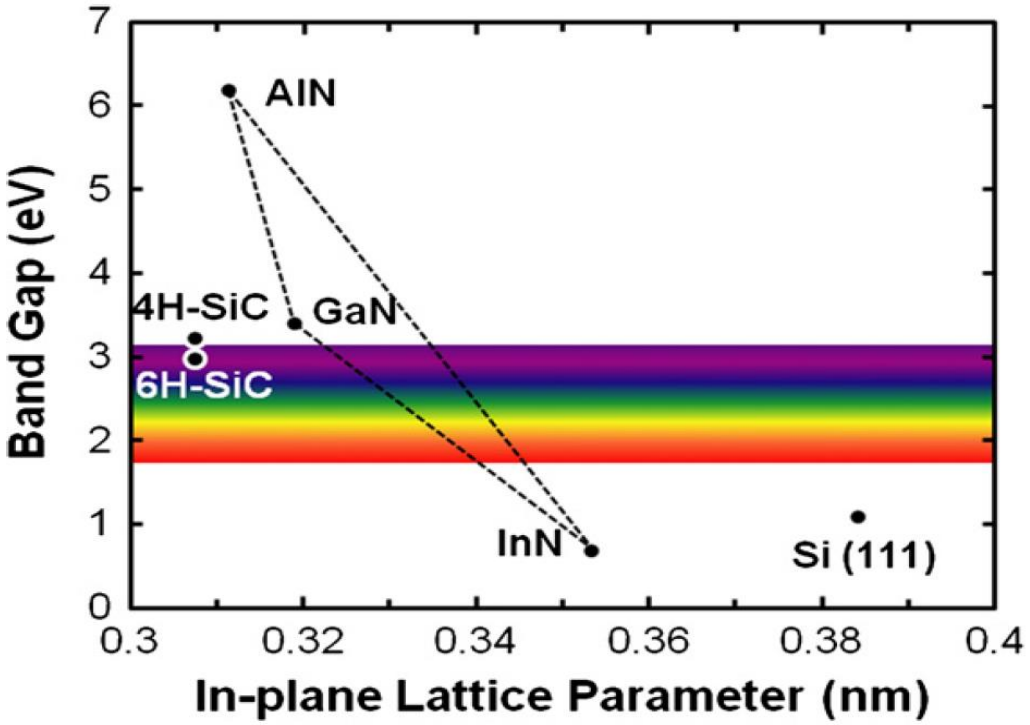


	GaN bulk	SiC	Al_2O_3 Sapphire	Si (111)
Lattice mismatch (%)	0	3.1	13	17
Thermal Conductivity (W/cmK)	2.3	4	0.3	1.48
Availability / Price				
Potential for high volume production				

Taken from S.W. Kaun, Semicond. Sci. Technol. 28 (2013) 074001

Substrates for GaN devices

Lattice matching of epi-layers, substrates



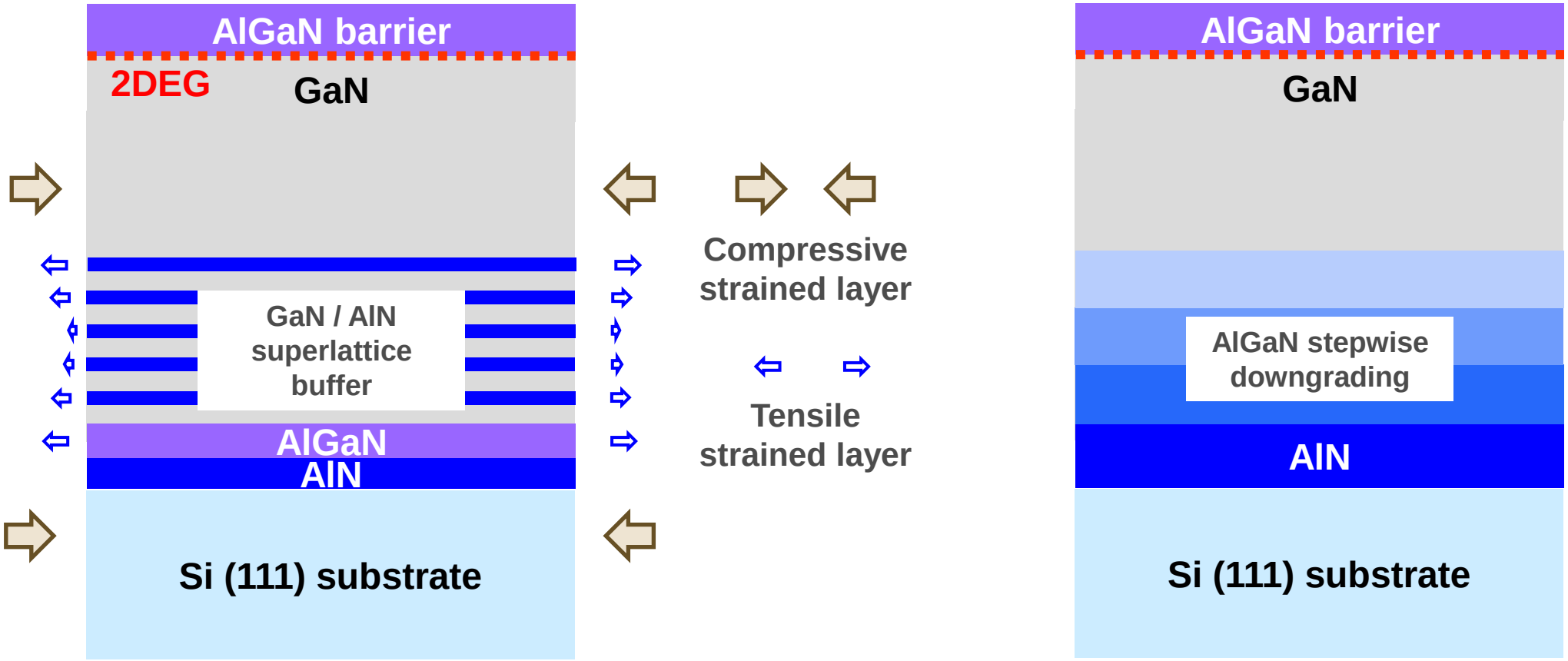
Taken from S.W. Kaun, Semicond. Sci. Technol. 28 (2013) 074001

High reliability microwave devices

	GaN bulk	SiC	Al_2O_3 Sapphire	Si (111)
Lattice mismatch (%)	0	3.1	13	17
Thermal Conductivity (W/cmK)	2.3	4	0.3	1.48
Availability / Price				
Potential for high volume production				

The driving force for high volume GaN-on-Si devices

GaN-on-Si epitaxy: Methods of strain compensation

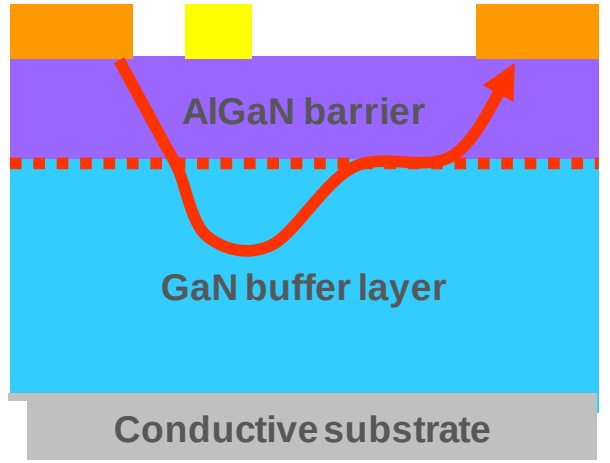


Left image: According to T. Ueda, "Recent advances and future prospects on GaN-based power devices," International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014, pp. 2075-2078, 18-21.

Epitaxial layers towards high breakdown devices

Avoid electron punch-through at high voltage pinch-off

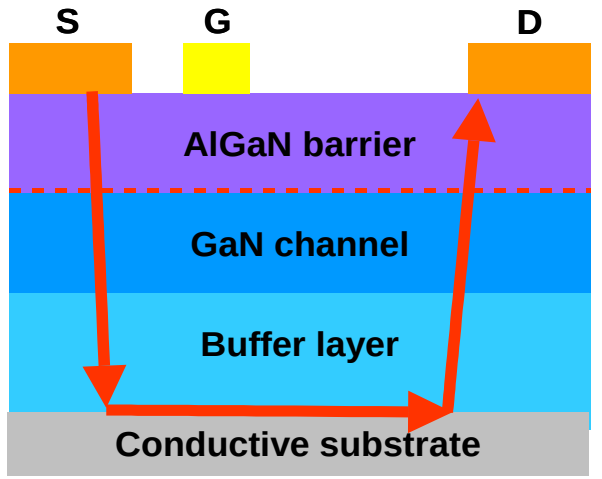
- →Confine electrons in channel



Punch-through effect

In case of conductive substrate:

- Avoid vertical breakdown



Vertical breakdown through buffer

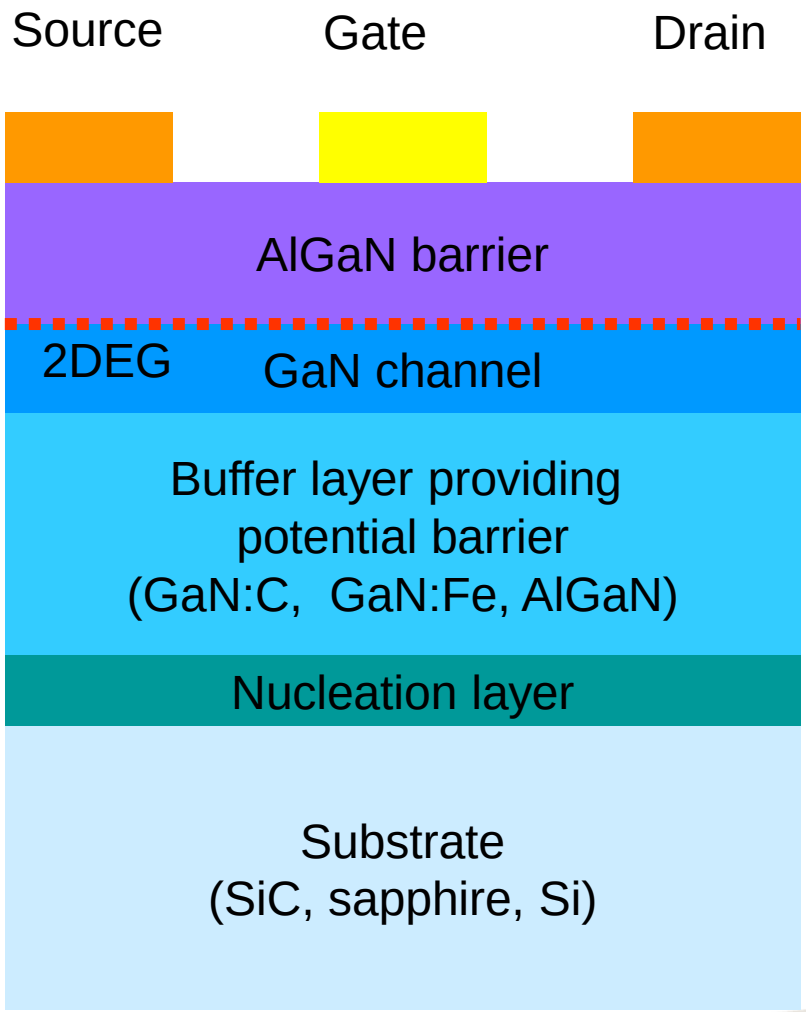
Optimization of epitaxial layer design (1): General considerations

Avoid electron punch-through at high voltage pinch-off

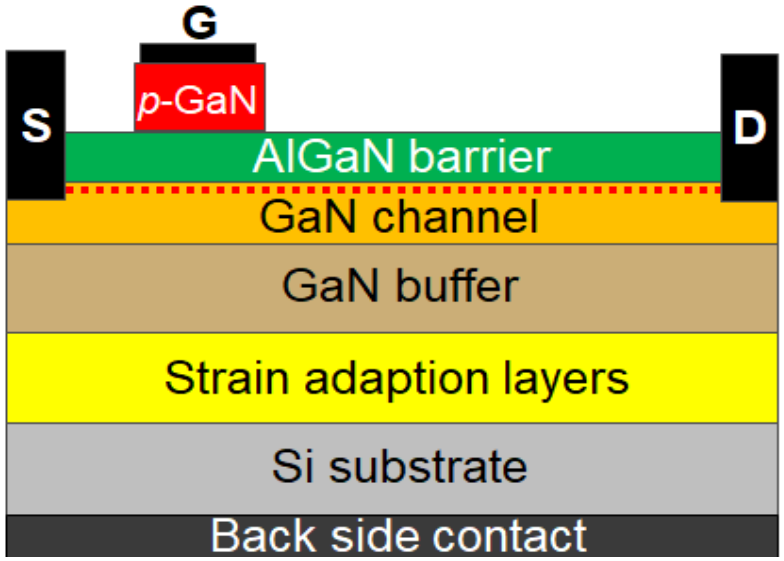
- → Confine electrons in channel
- → Provide suitable potential barriers
  - AlGaN-buffer
  - C-, Fe- doping….

In case of conductive substrate:

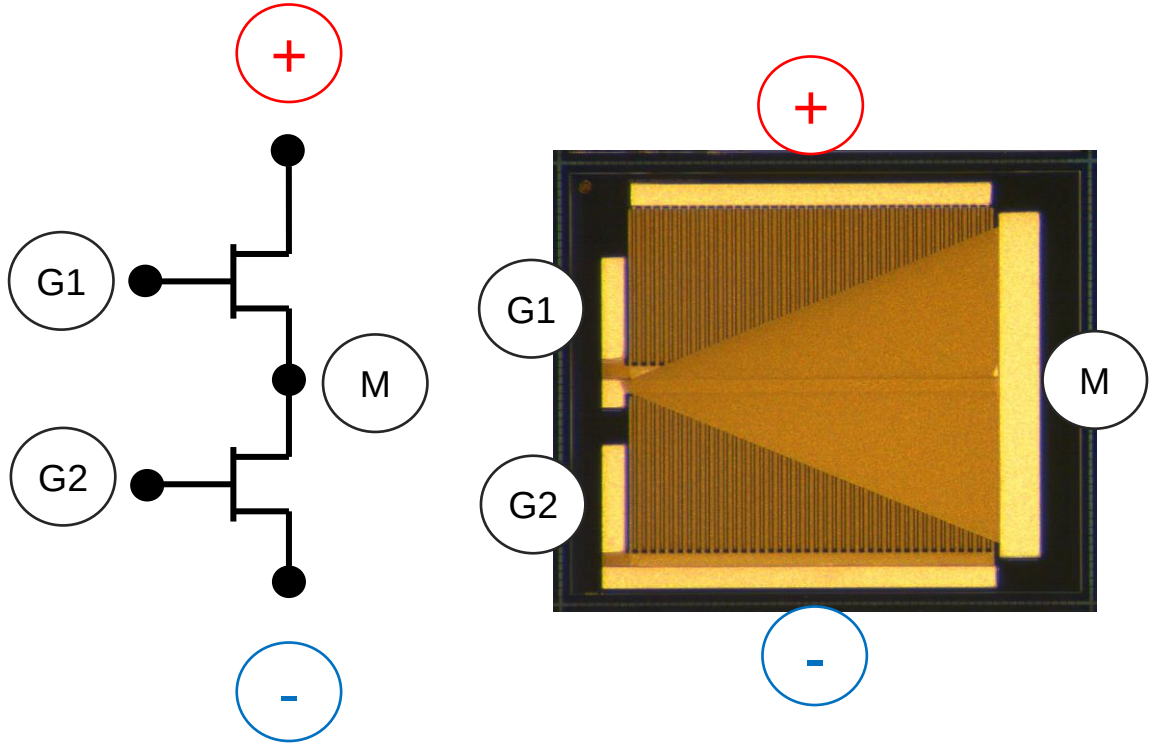
- Avoid vertical breakdown
- Use proper buffer material and thickness



FBH p-GaN normally-off technology (1)



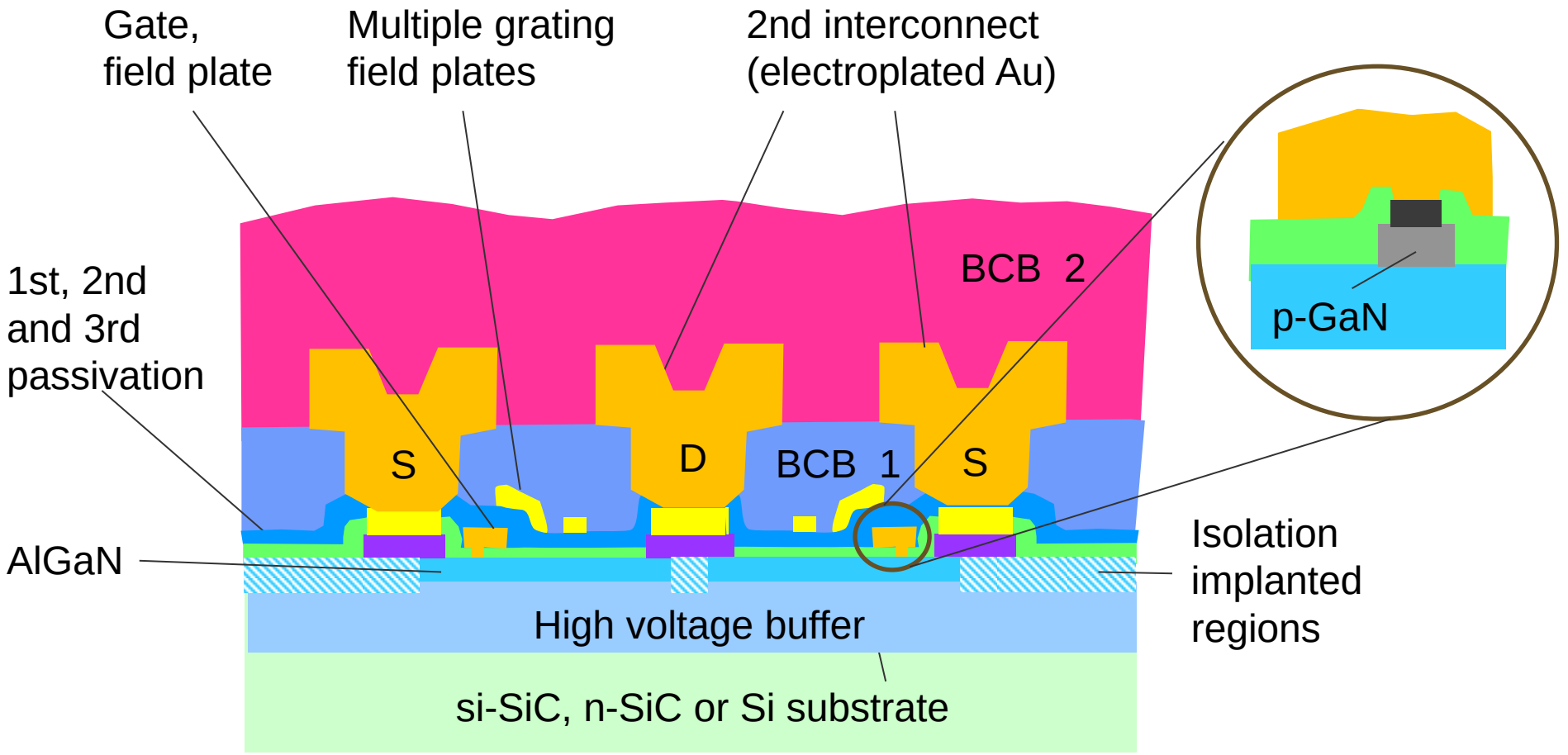
GaN-on-Si HFET



Example: Monolithically integrated half-bridge

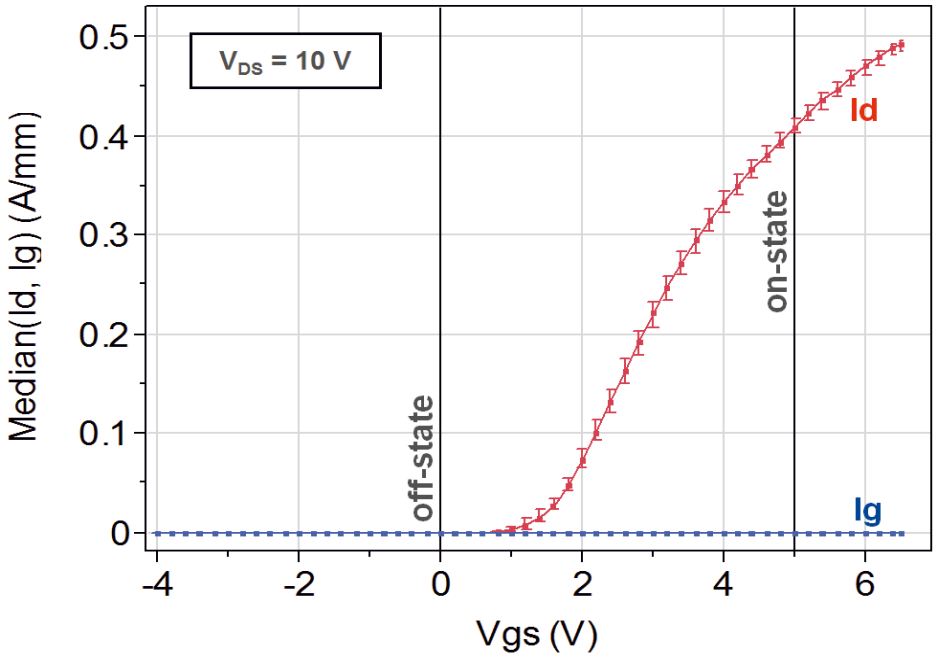
- Normally-off technology, threshold about +1 V
- Designed for 60 mΩ on-state resistance
- 600 V switching capability

FBH p-GaN normally-off technology (2)

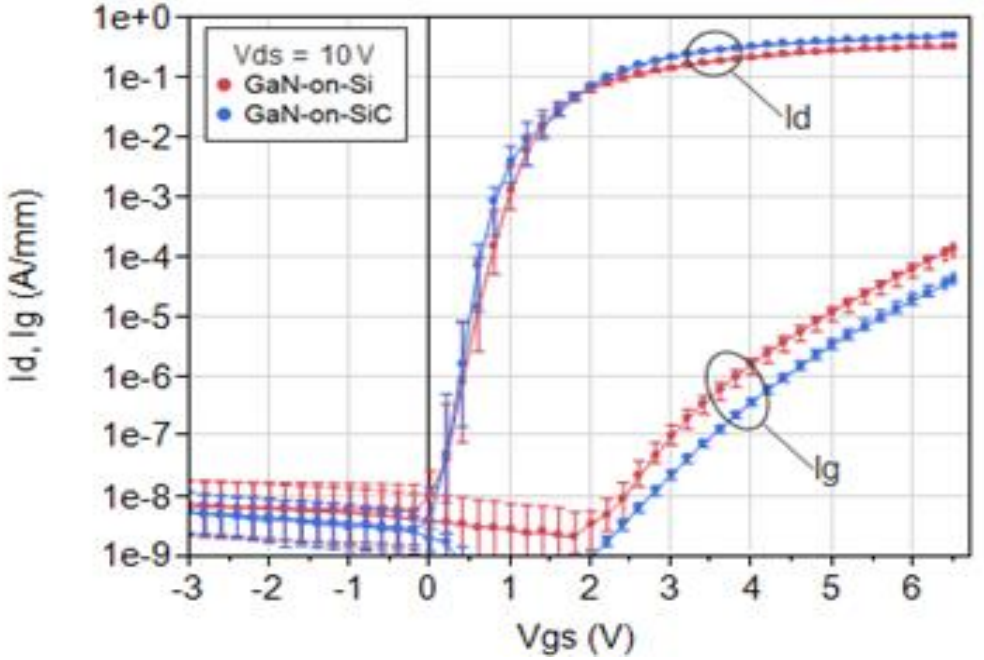


60 mΩ, 600 V normally-off Devices: normally-off properties

- Device periphery 214 mm, GaN-on-SiC
- Chip size: 9 mm²
- Threshold voltage +1.5 V



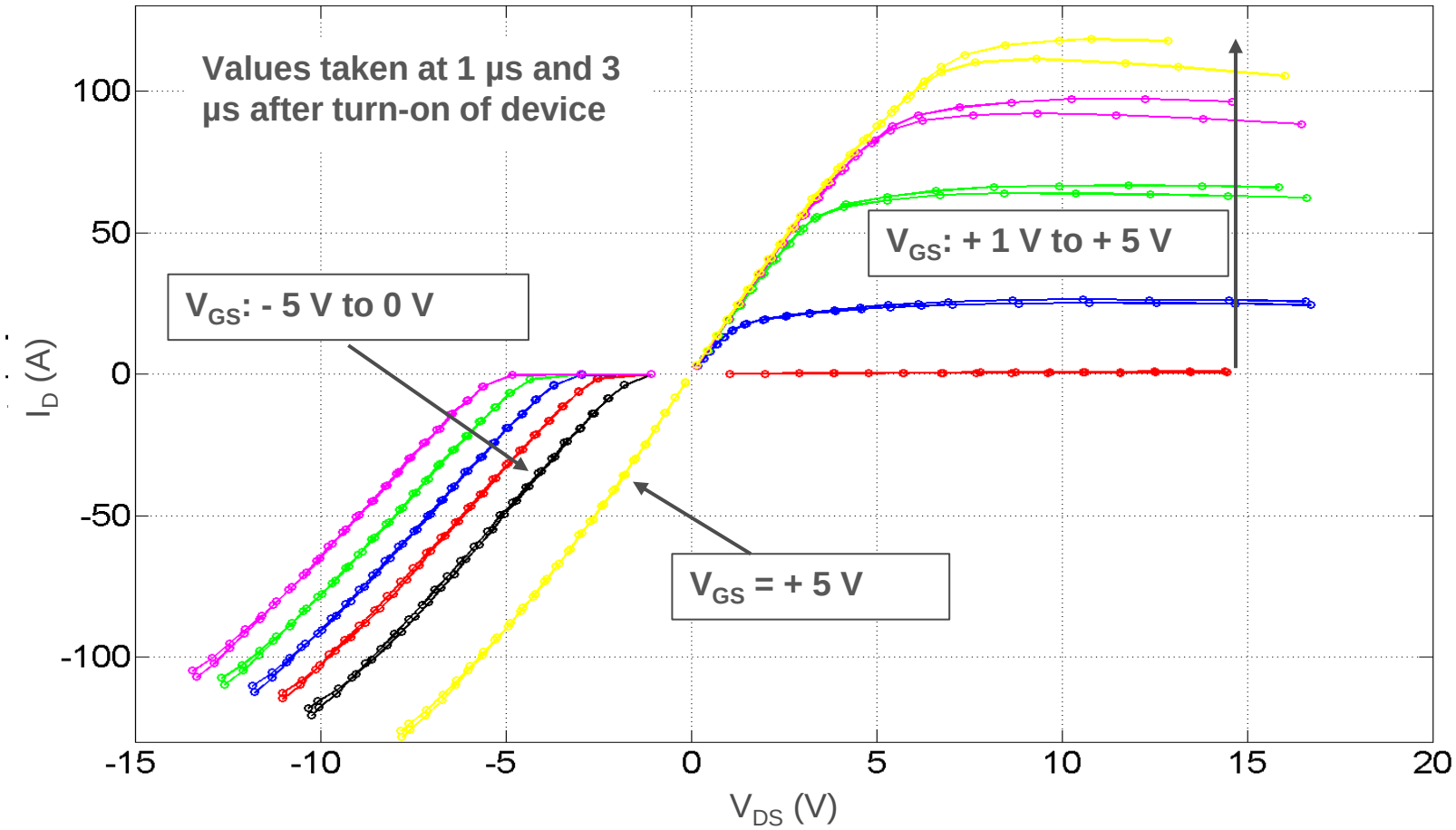
Transfer characteristics (linear)



Transfer characteristics (half log)

- Good turn-off at 0 V gate bias
- Maximum current 120 A

Bi-directional operation capability



- Devices also operate in reverse mode
- This feature might be implemented in novel system / circuit architectures

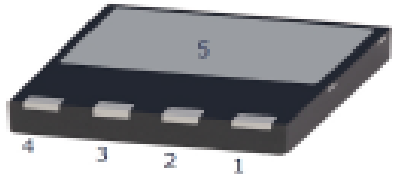
Comparison FBH power GaN vs. Infineon CoolMOS

FBH GaN normally-off device

	FBH GaN normally-off 600 V / 60 mΩ	Infineon CoolMOS*
C_{ISS} (300 V)	90 pF	3000 pF
C_{OSS} (300 V)	35 pF	50 pF
C_{RSS} (300 V)	2.5 pF	6 pF
E_{OSS} (400 V)	5 µJ	8 µJ
Q_G (100 V)	15 nC	64 nC
R_{ON} x Q_G	0.98 nCΩ	4.5 nCΩ

*): 650 V 70 mΩ C7 CoolMOS in ThinPAK, Infineon IPL65R070C7

Infineon CoolMOS



Gate charge and R_{on} x Q_G reduced by a factor of 5

- Compared on the basis of nominally the same operation current, on-state resistance and voltage capability
- Significantly reduced input capacitance, feed-back capacitance comparable

Comparison FBH power GaN vs. Infineon CoolMOS

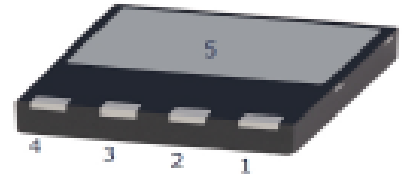
FBH GaN normally-off device

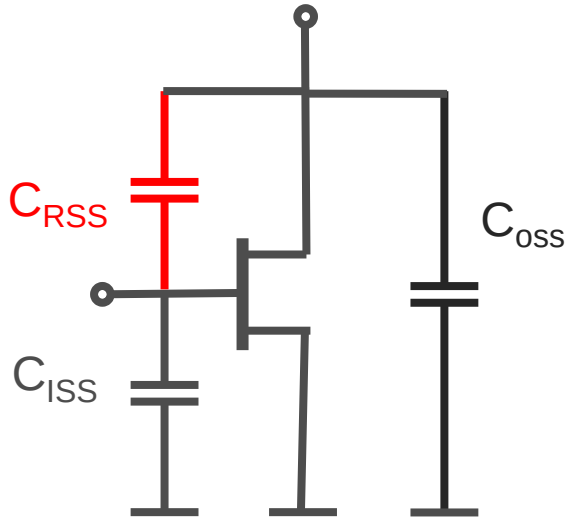
	FBH GaN normally-off 600 V / 60 mΩ	Infineon CoolMOS*
C_{ISS} (300 V)	90 pF	3000 pF
C_{OSS} (300 V)	35 pF	50 pF
C_{RSS} (300 V)	2.5 pF	6 pF
E_{OSS} (400 V)	5 µJ	8 µJ
Q_G (100 V)	15 nC	64 nC
R_{ON} x Q_G	0.98 nCΩ	4.5 nCΩ

*): 650 V 70 mΩ C7 CoolMOS in ThinPAK, Infineon IPL65R070C7

Gate charge and R_{on} x Q_G reduced by a factor of 5

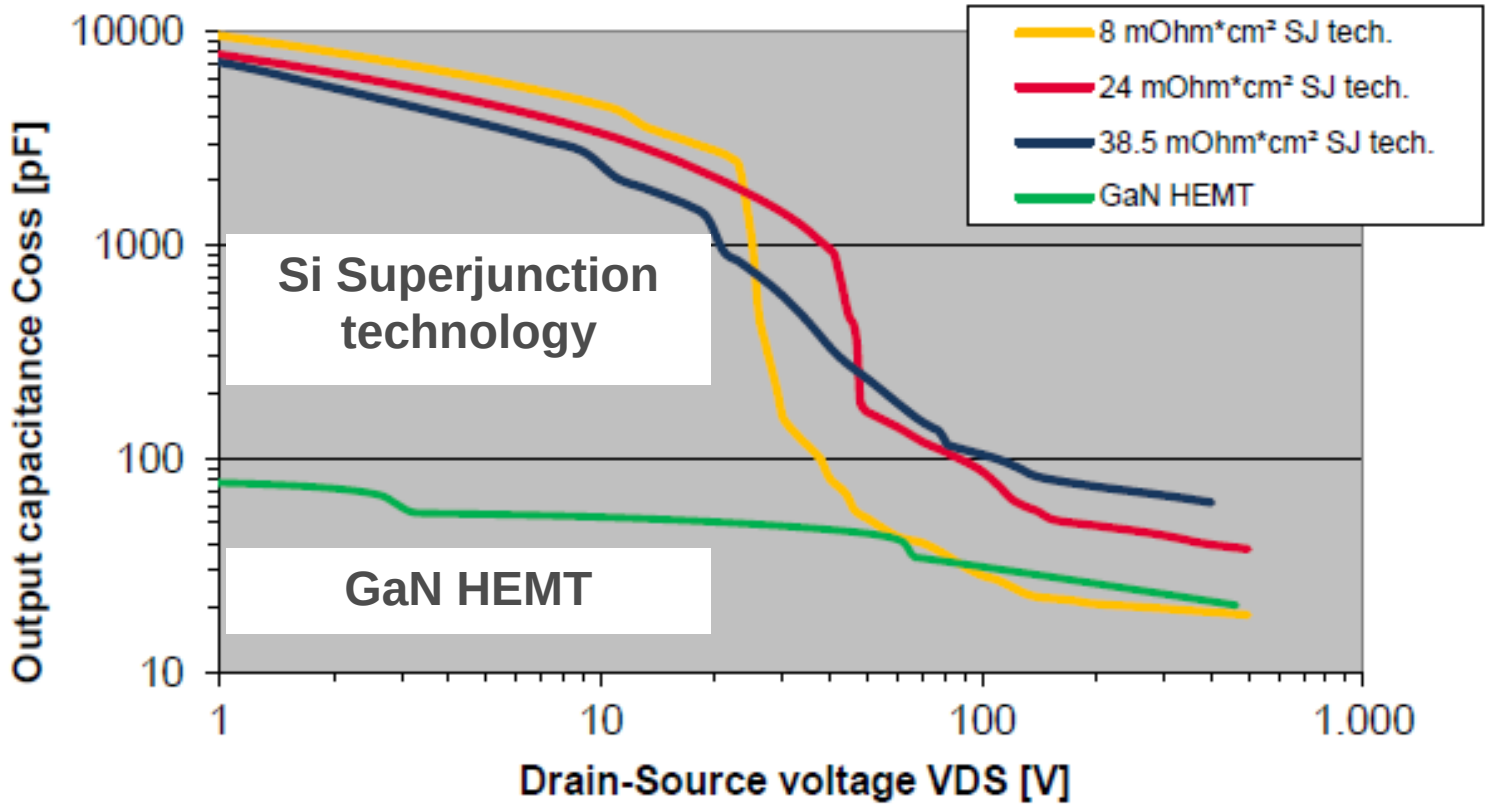
Infineon CoolMOS

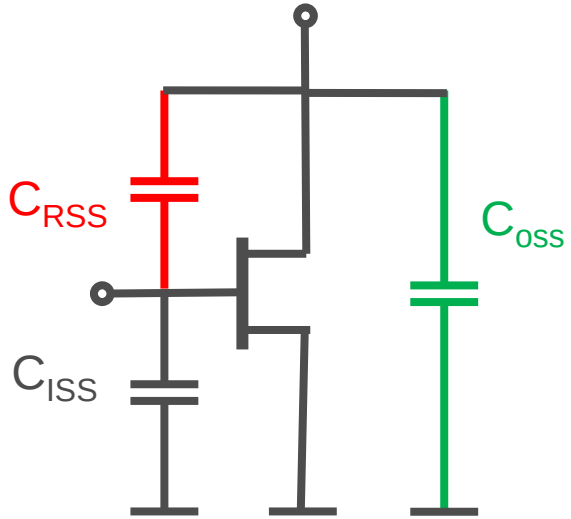




- Compared on the basis of nominally the same operation current, on-state resistance and voltage capability
- Significantly reduced input capacitance, feed-back capacitance comparable

GaN vs. CoolMOS: Output capacitance

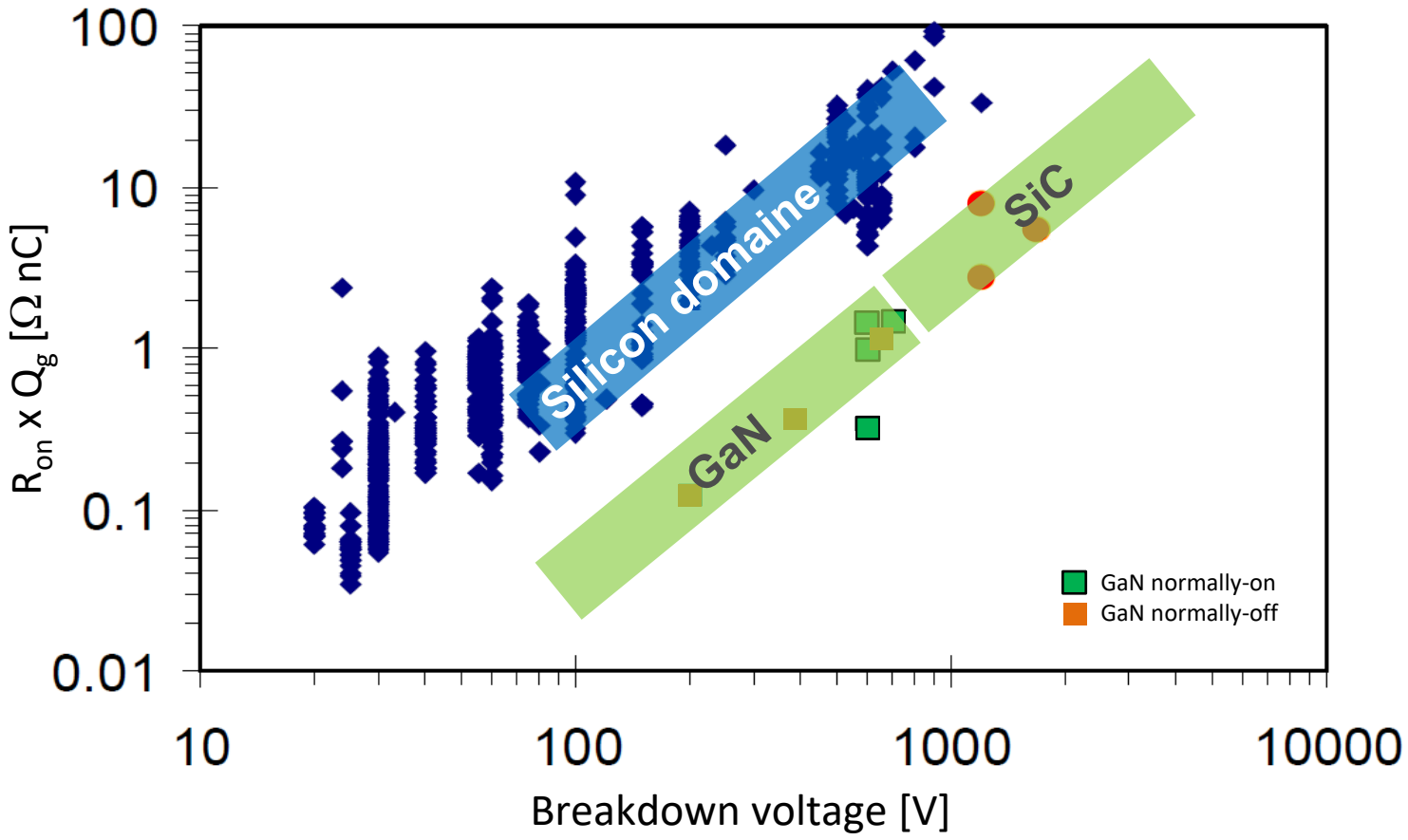




- Small variation of GaN output capacitance with drain voltage

G. Deboy, IEDM 2016, pp 532-535

New GaN devices promise fast and efficient power switches



R_{on} x Q_g:

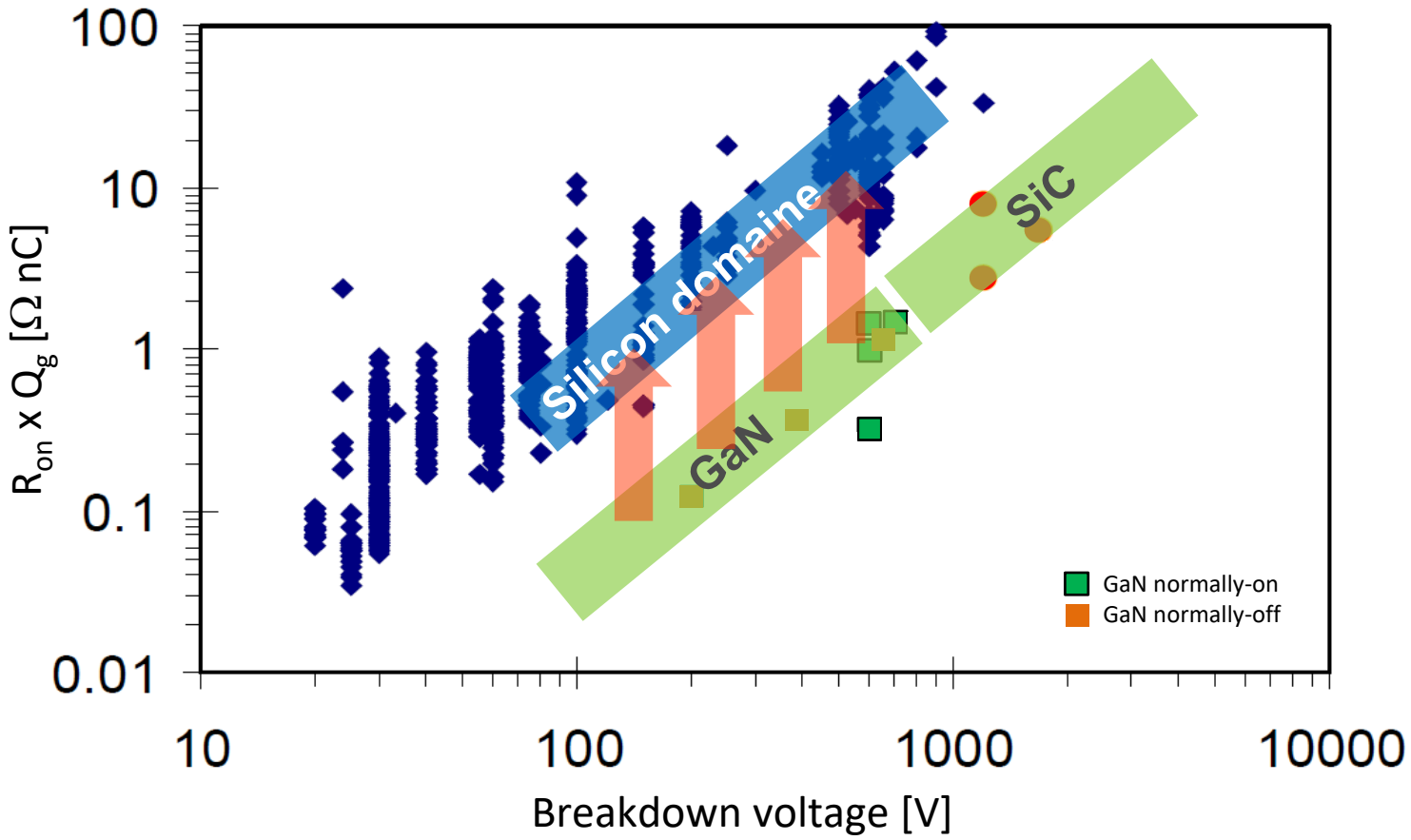
- measure for efficient switching properties

Requirements for efficient switches:

- Low dynamic on-state resistance
- Small gate charge

Leibniz Ferdinand Braun Institut

New GaN devices promise fast and efficient power switches



R_{on} x Q_g:

- measure for efficient switching properties

Requirements for efficient switches:

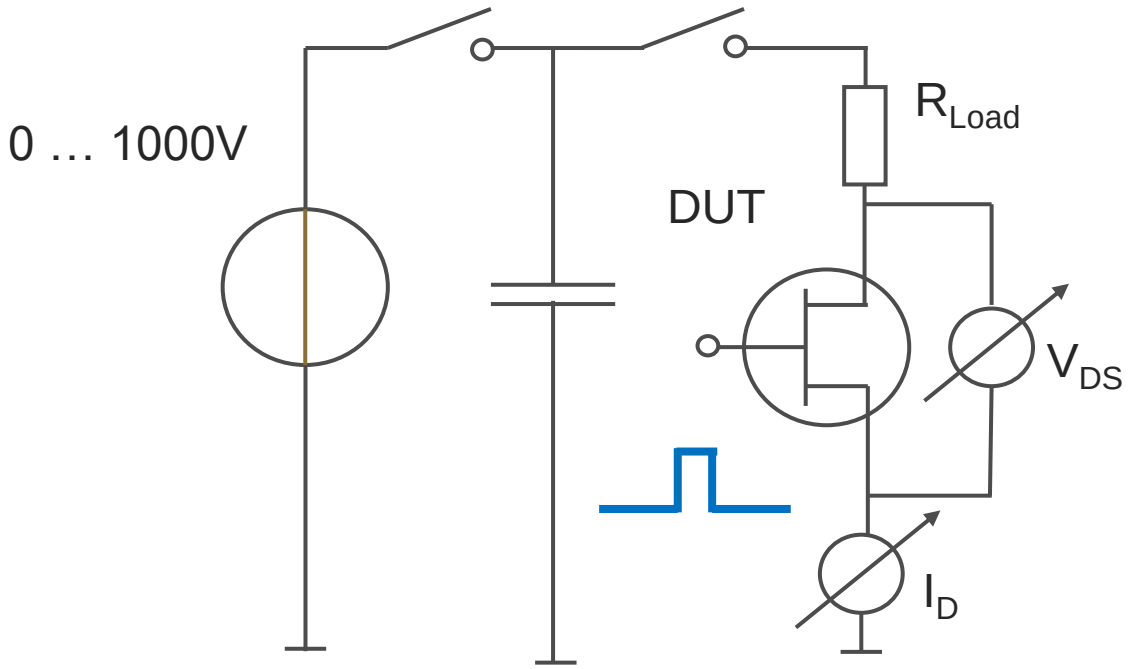
- Low dynamic on-state resistance
- Small gate charge

Dynamic effects temporary increase on-state resistance

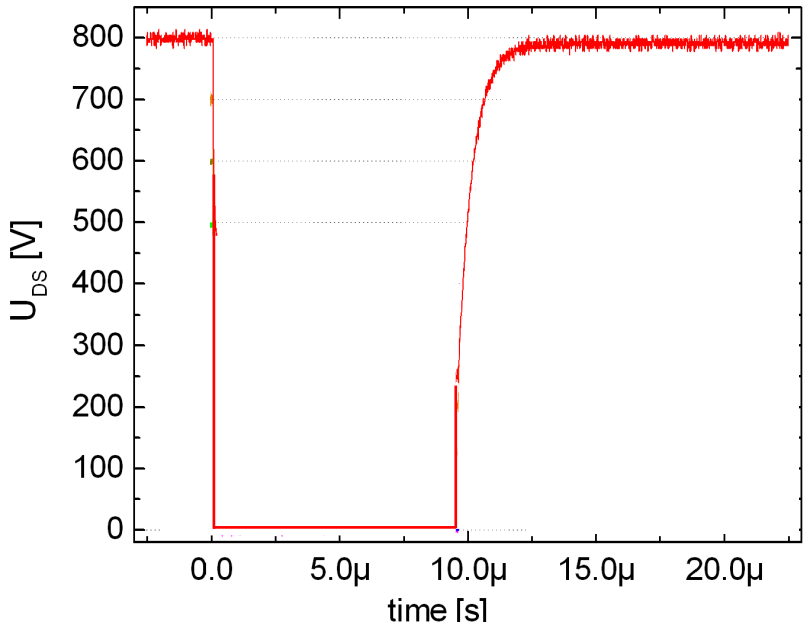
This needs to be understood and harnessed

Leibniz Ferdinand Braun Institut

Dynamic on-state resistance increase after high voltage switching: Measurement principle

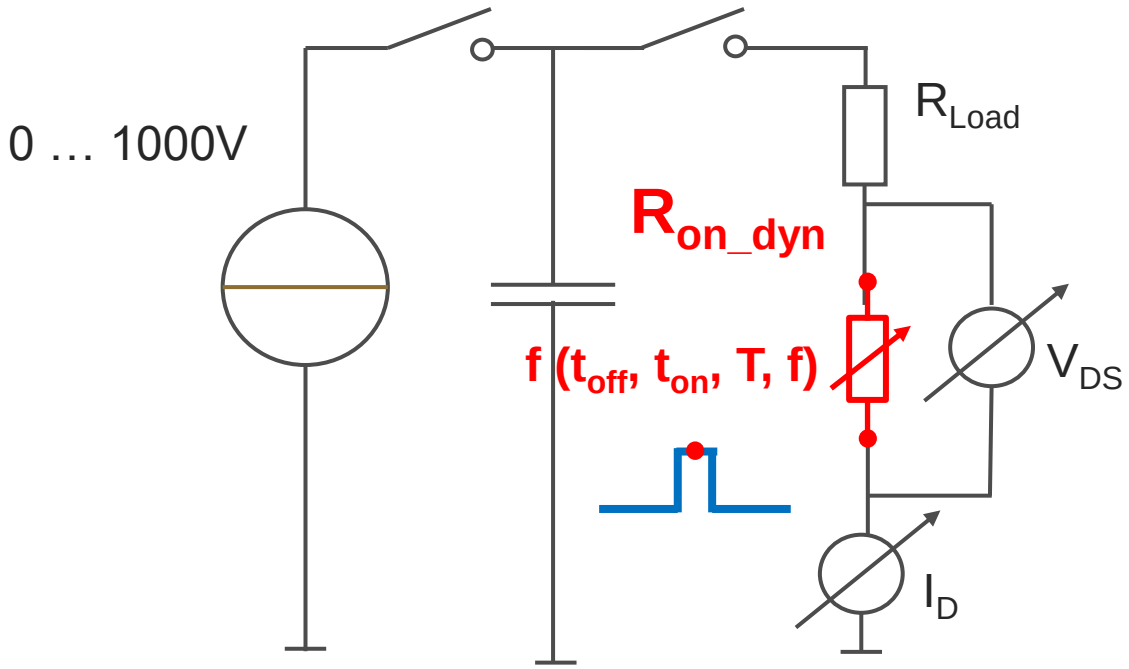


Test set-up for measuring dynamic Ron



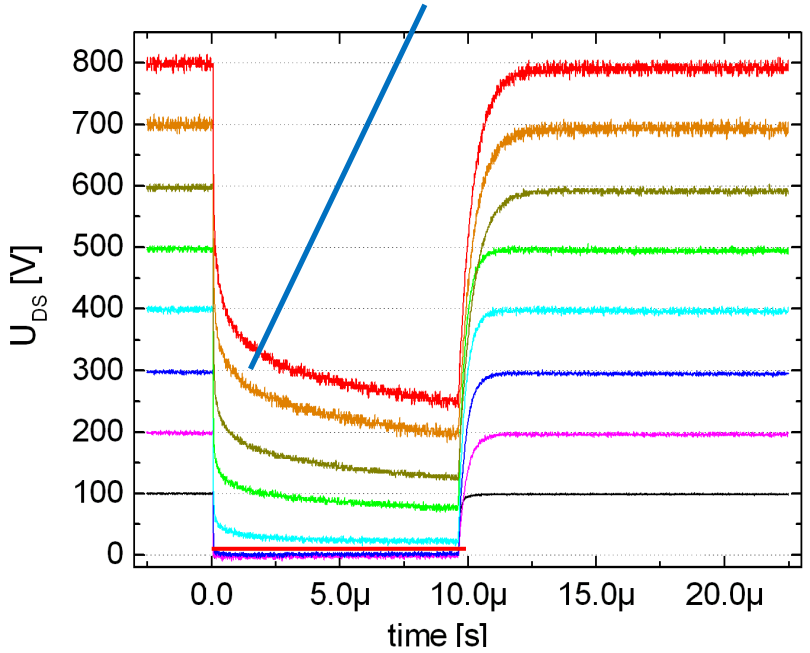
High voltage switching tests (practically ideal devices)

Dynamic on-state resistance increase after high voltage switching: Measurement principle



Test set-up for measuring dynamic Ron

Pronounced on-state voltage drop due to increased dynamic on-state resistance



High voltage switching tests (early devices)

Dynamic on-state resistance: Physics behind

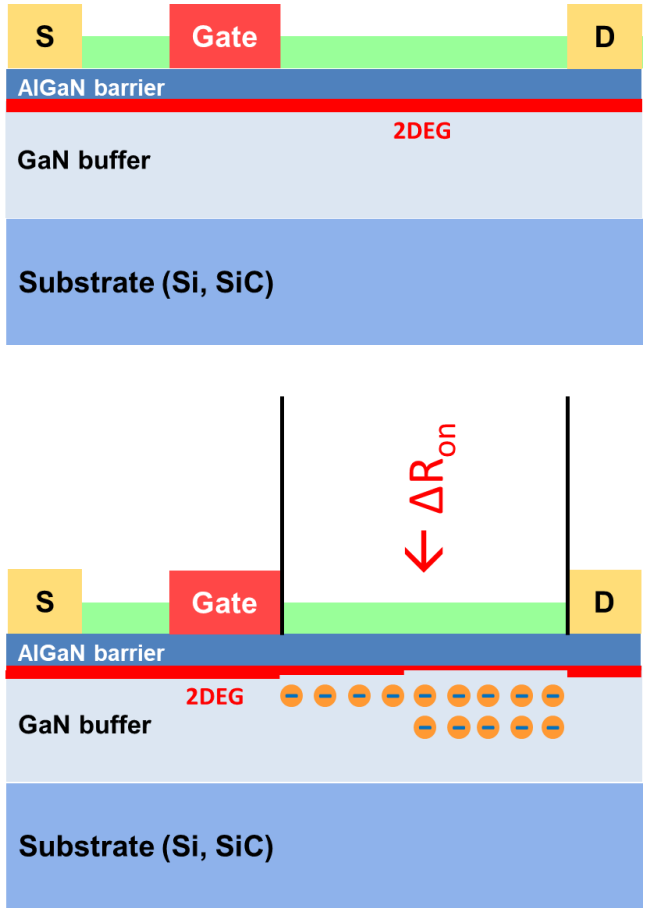
Appearance of negative charges next to 2DEG as a consequence of device biasing history

- In semiconductor and passivation layer(s)
- Due to electron trapping after off-state biasing
- Due to release of deep acceptors

Dynamics of trapping depends on:

- Biasing conditions
  - Maximum bias voltage
  - Backside (substrate) potential
- Timing of on- and off-state biasing
  - Off state time (→ trapping)
  - On-state time (→ de-trapping)
  - Continuous switching
- Temperature

Therefore: Device mission profile is decisive



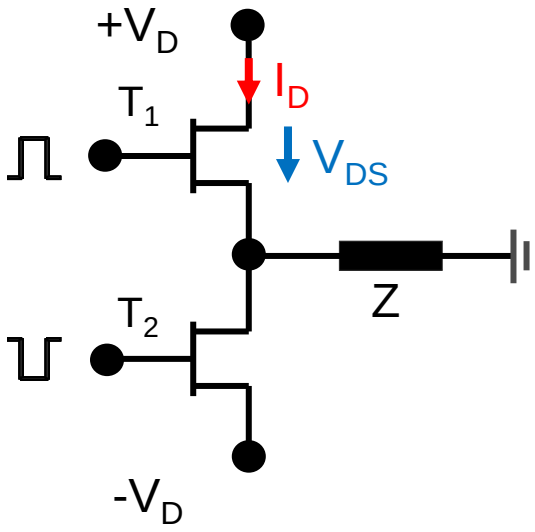
Ideal device:

No trapping effects

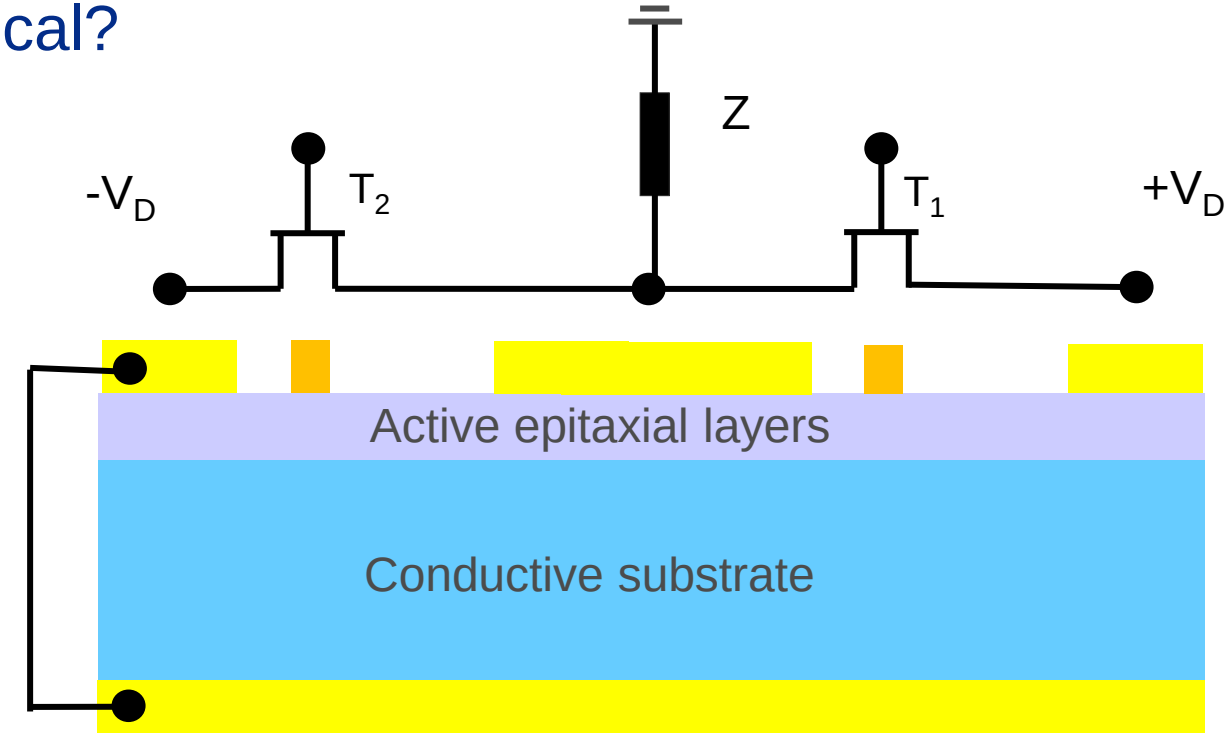
Real device:

Trapped negative charges close to 2DEG

Back-gating: Why is it critical?

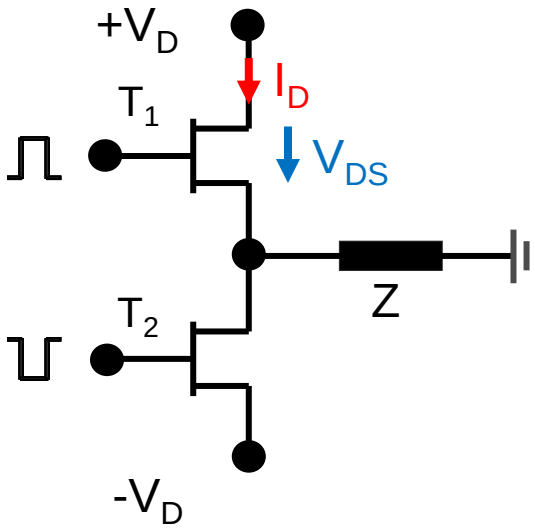


Half-bridge topology

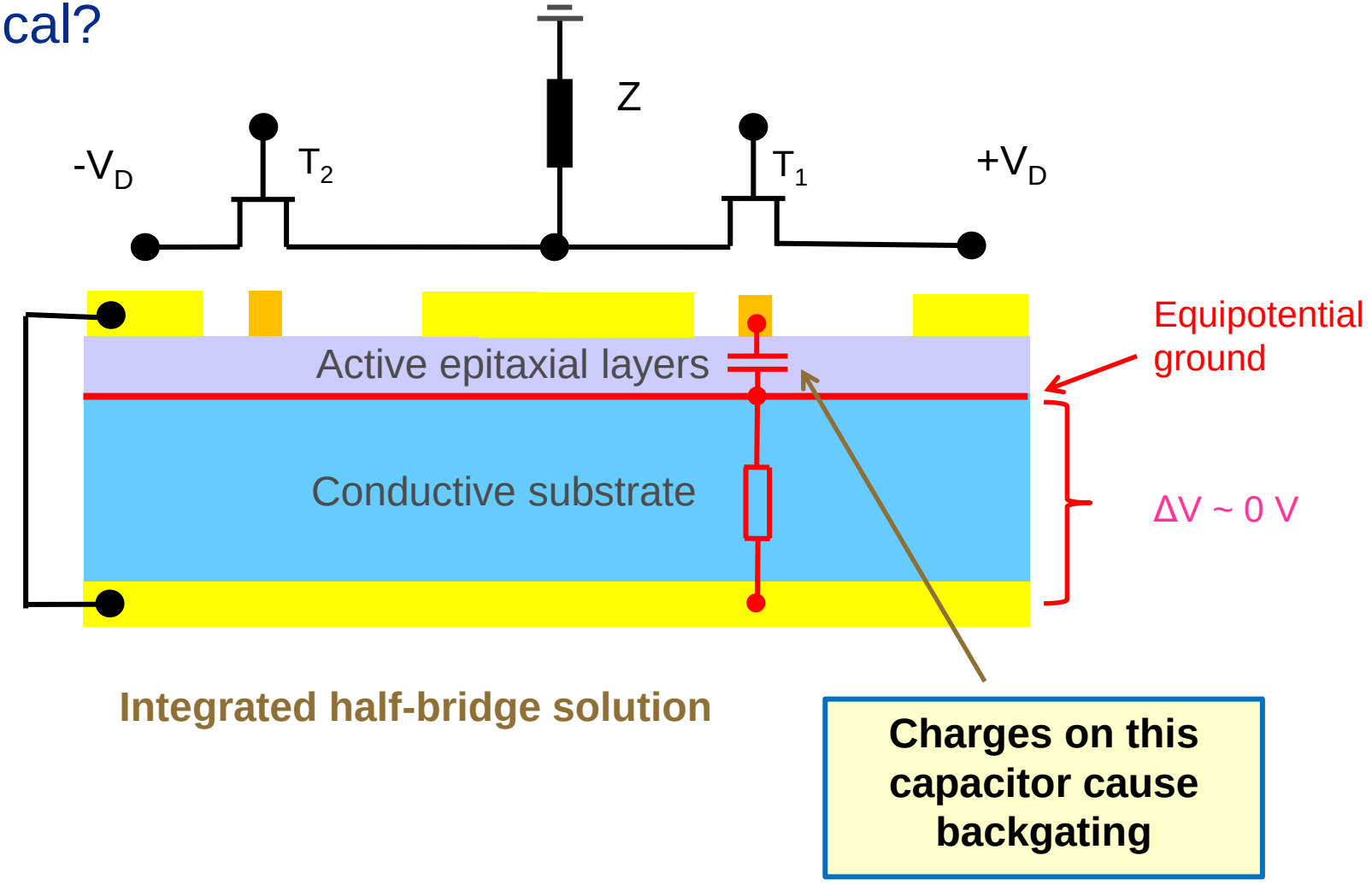


Integrated half-bridge solution

Back-gating: Why is it critical?

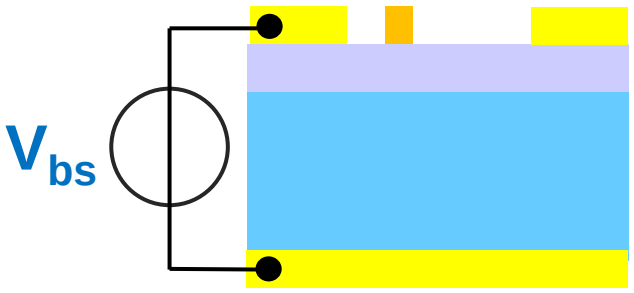


Half-bridge topology

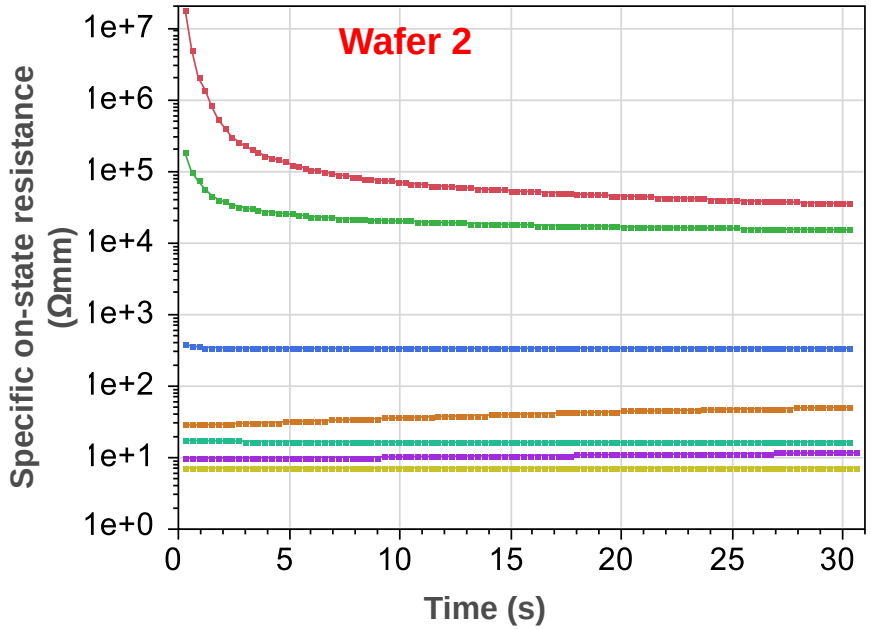


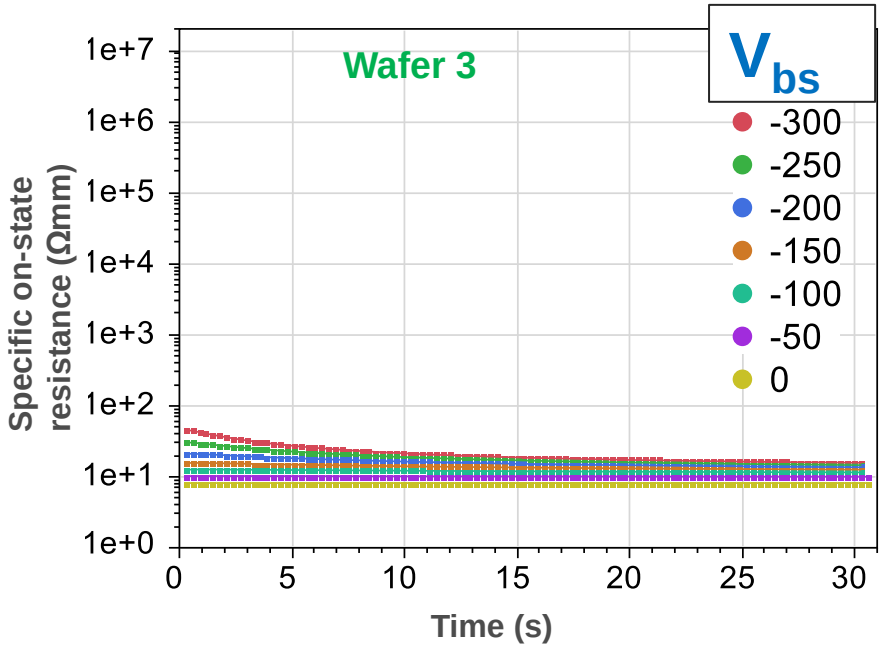
Integrated half-bridge solution

Back-gating and trapping after backside potential change



Back-gating test scheme

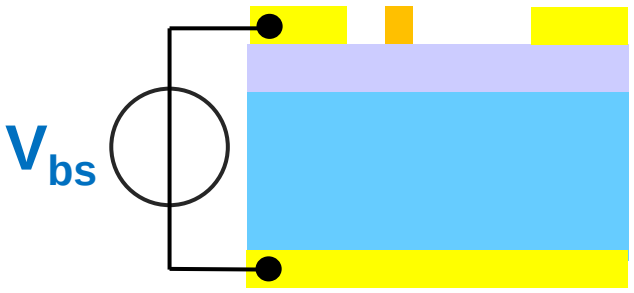




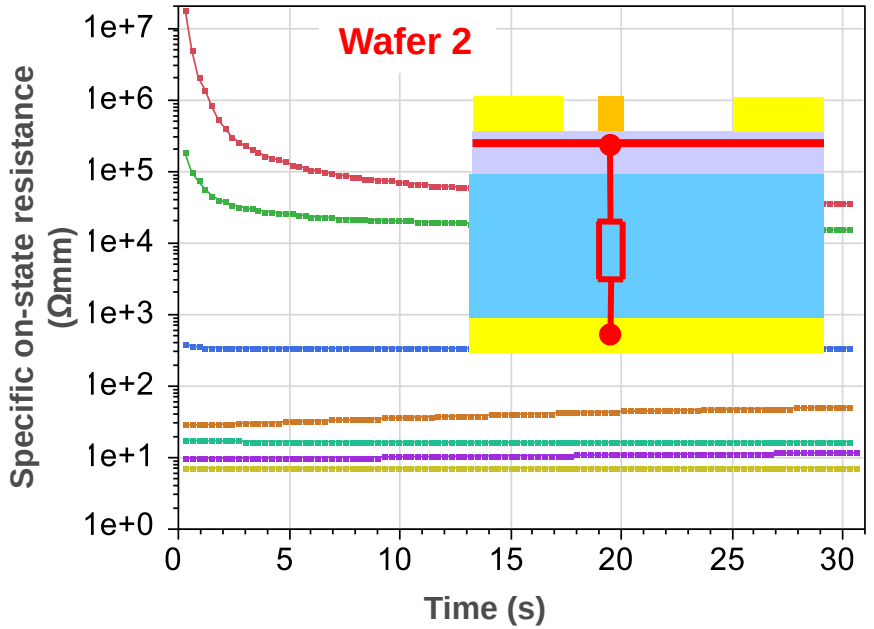
Integrated half-bridge switching: A problem which is not yet really solved

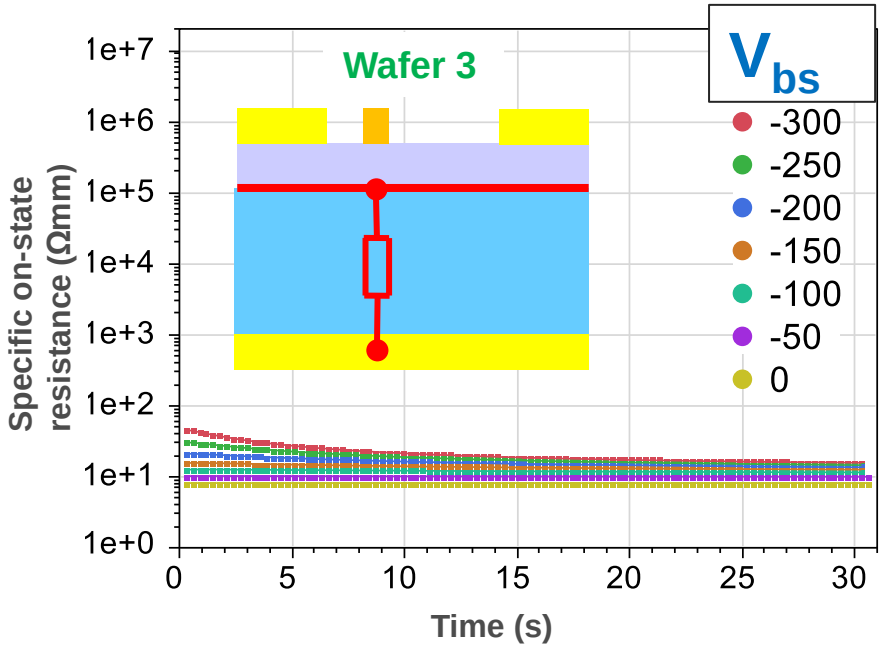
- Source of top transistor changes potential after turn-on of bottom transistor
  - Causes static back-gating and dynamic effects
  - Different finger prints of epi-technologies observable

Back-gating and trapping after backside potential change



Back-gating test scheme





Integrated half-bridge switching:
A problem which is not yet really solved

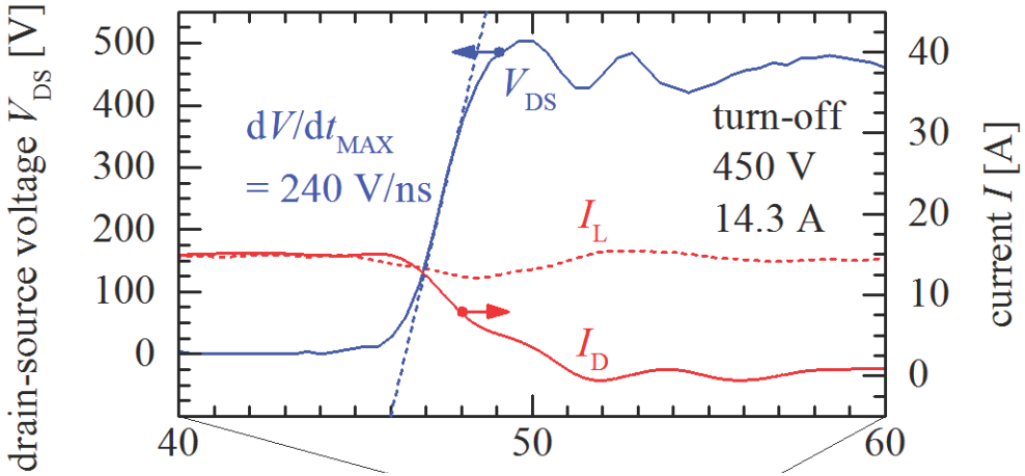
- Source of top transistor changes potential after turn-on of bottom transistor
  - Causes static back-gating and dynamic effects
  - Different finger prints of epi-technologies observable

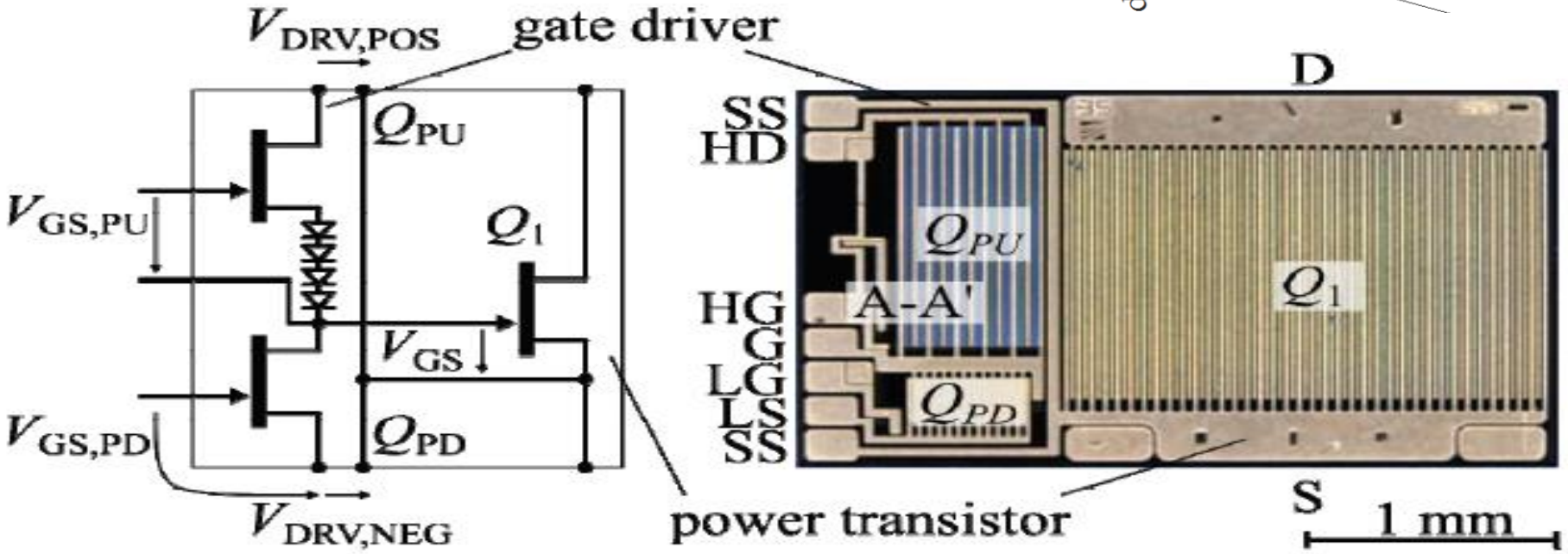
Effective equipotential ground position differs from epi to epi

Monolithically integrated driver solutions

Motivation

- To reduce parasitic inductivities
- To realize faster and more precise switching

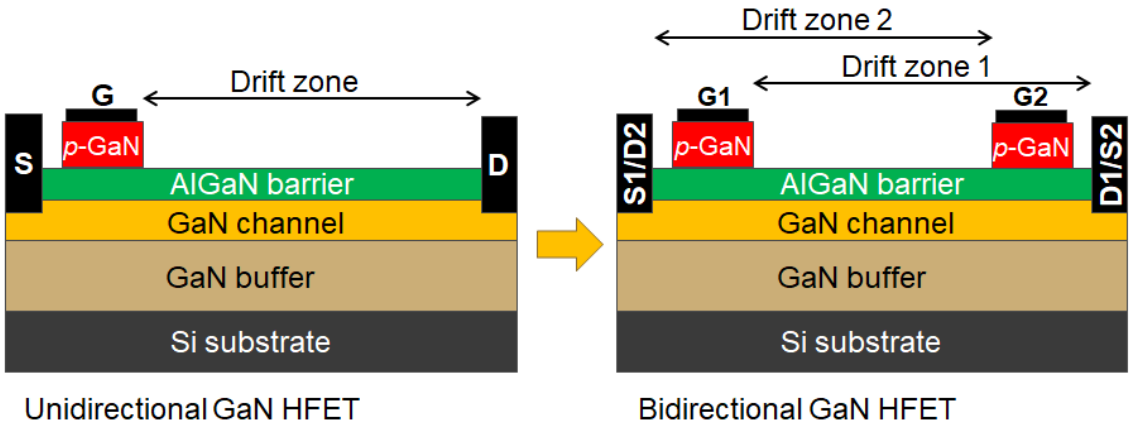




S. Moench et al.: 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2015, pp. 92-97.

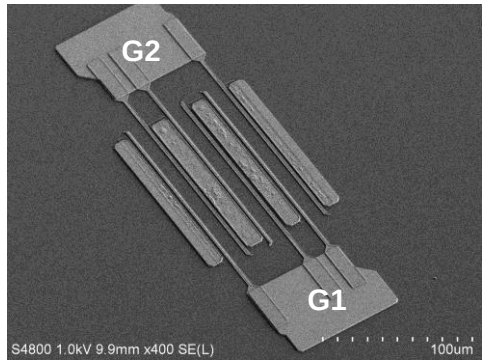
Bidirectional 600 V GaN HFETs

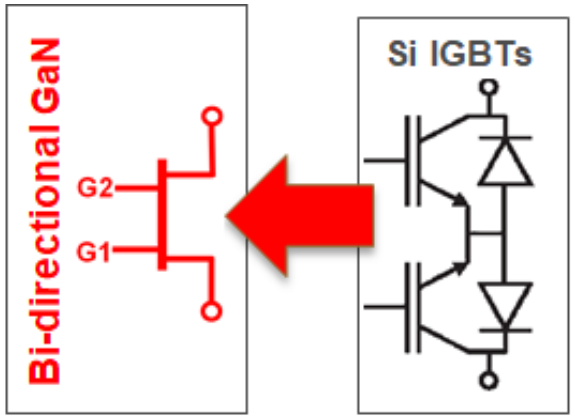
- 600 V device with bidirectional functionality
  - Matrix converter for direct AC-AC conversion
  - T-type converter for DC-AC conversion
- Double R_{ON} in (Si-based) vertical 600 V technology
- GaN HFET integration
  - One drift region used for both directions



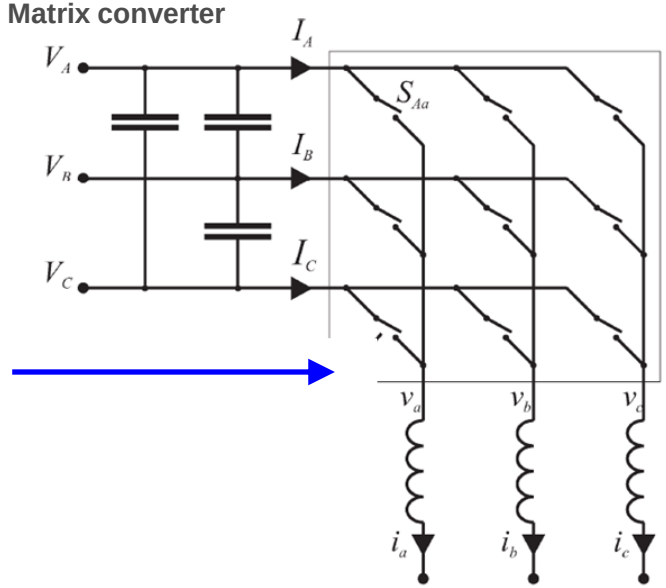
Unidirectional GaN HFET

Bidirectional GaN HFET

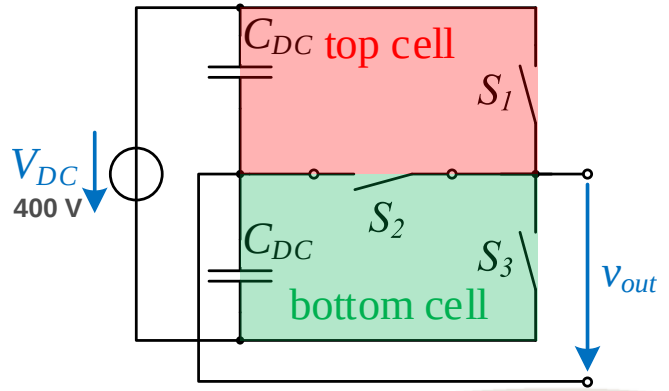




Matrix converter



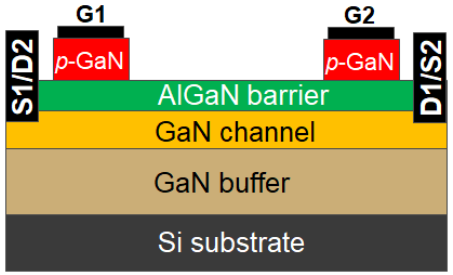
T-type converter

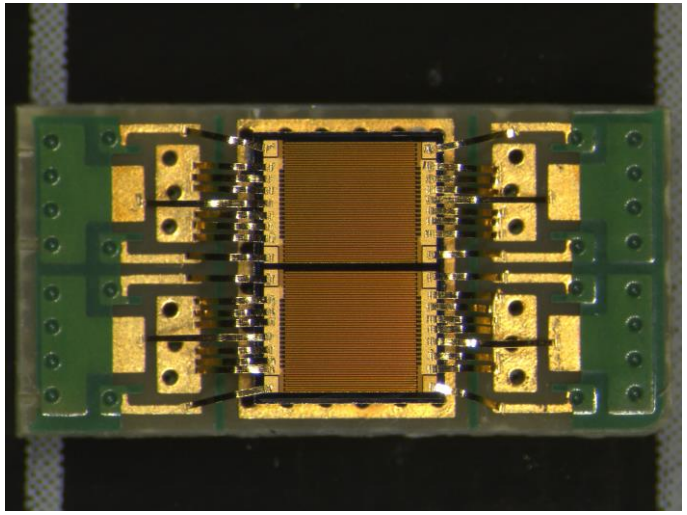


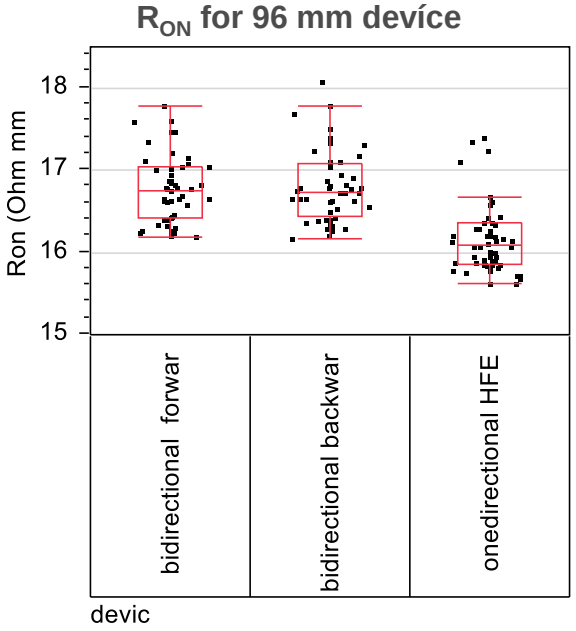
Leibniz Ferdinand Braun Institut

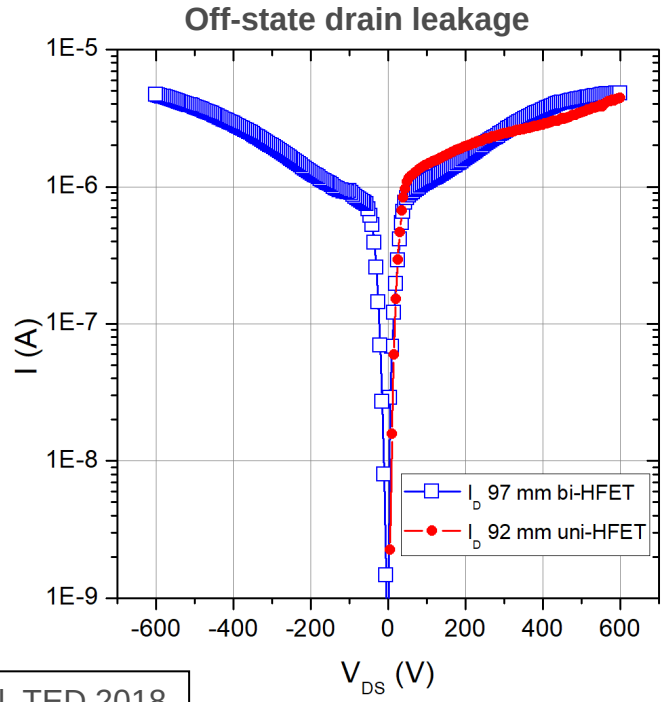
Bidirectional 180 mΩ / 600 V GaN HFET

- 600 V device with bidirectional functionality
- 5% larger R_{ON} as for unidirectional HFET
- Symmetrical switching transients

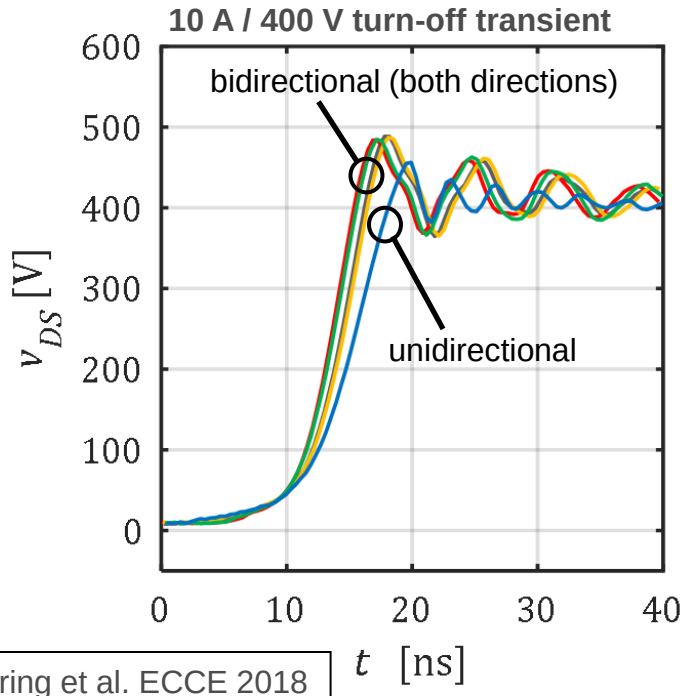








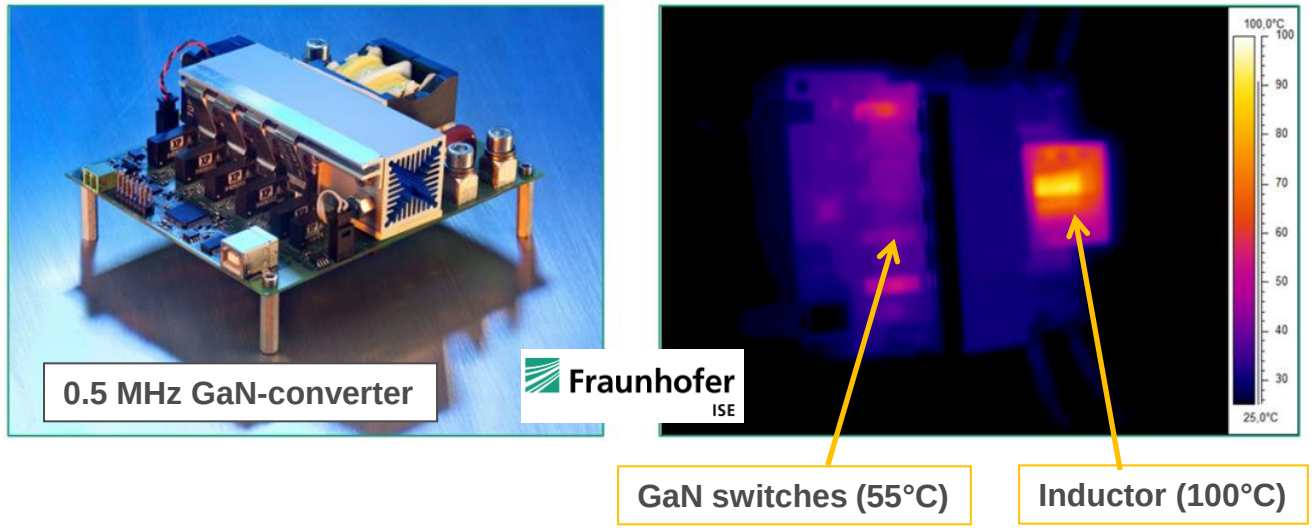
M. Wolf et al. TED 2018



C. Kuring et al. ECCE 2018

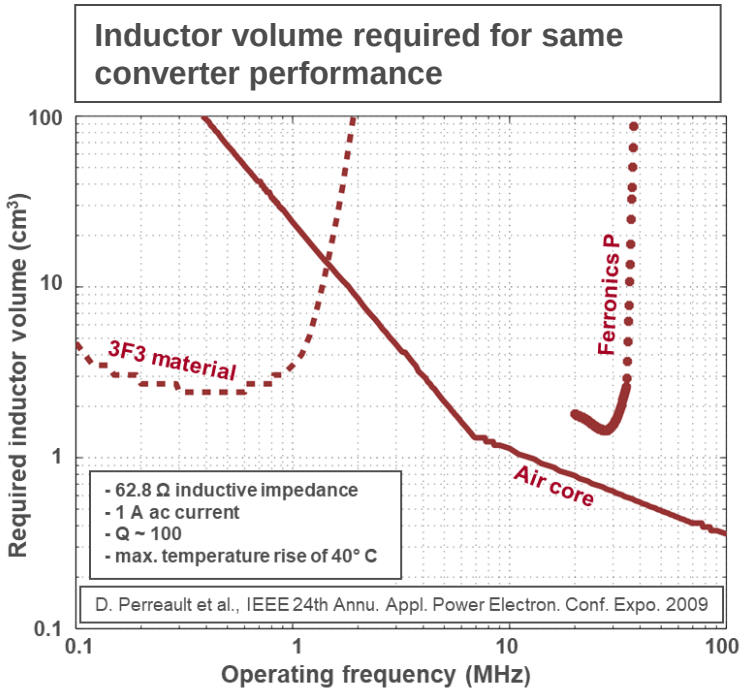
Losses in fast switching power converters

Also passives have switching losses



- Low transistor switching losses thanks to GaN
  → higher switching frequency

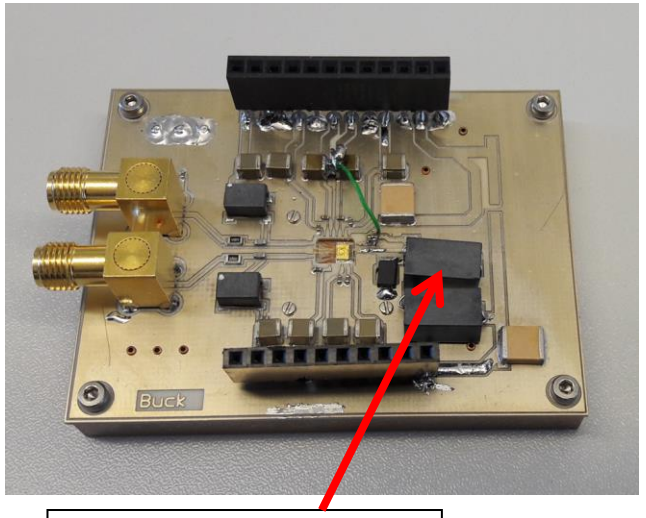
→ Ferrite core inductor magnetizing losses increase with frequency
  – Magnetizing losses eventually dominate



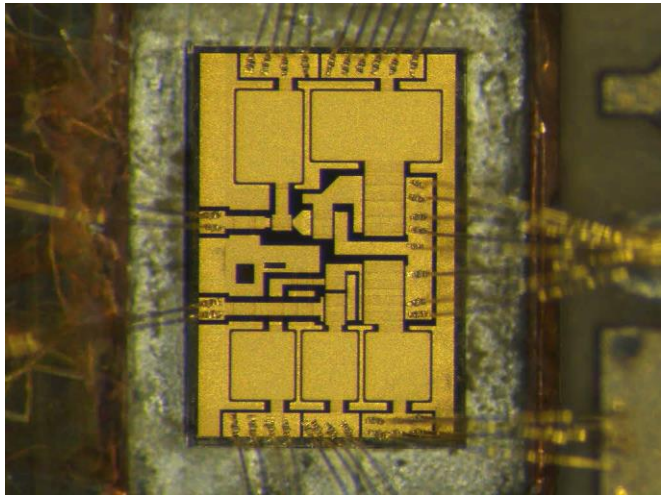
- Air core inductors have low inductance per volume but no magnitizing losses
- Air core inductors need less volume for converter frequencies > 10 MHz

VHF converter with Fe-free inductor

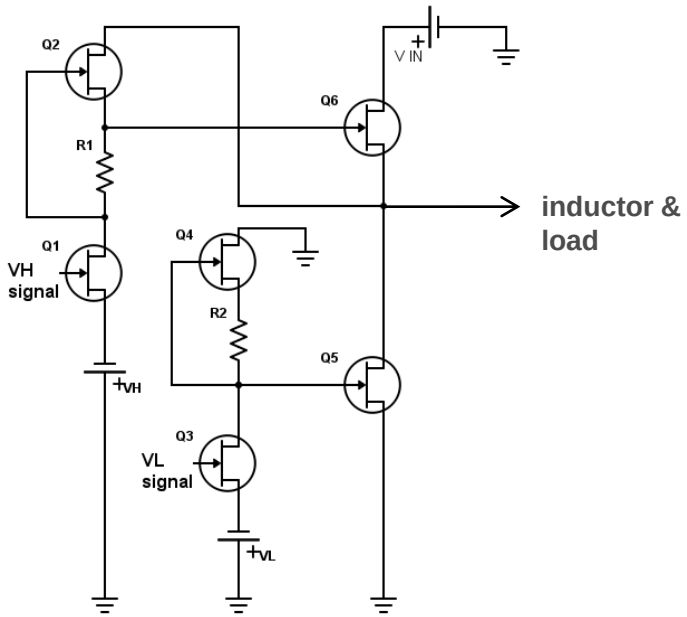
- Half bridge and gate drivers on one chip (FBH 0.25 µm GaN MMIC process)
- 100 MHz switching frequency
- No coils with magnetic materials → **air coils**
- 87% power efficiency for 30 V / 14.5 W



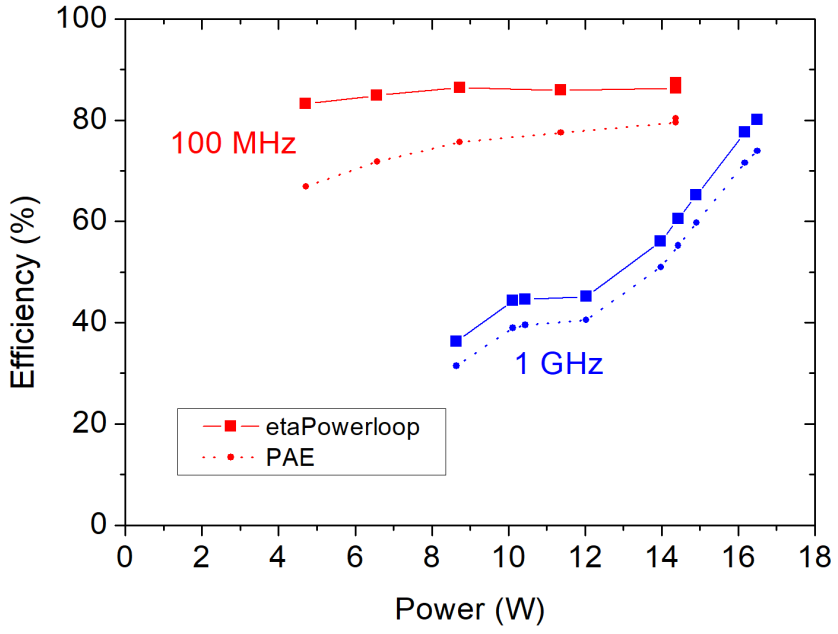
2 air coils à 0.5 µH



Chip size: 2.5 x 1.7 mm²

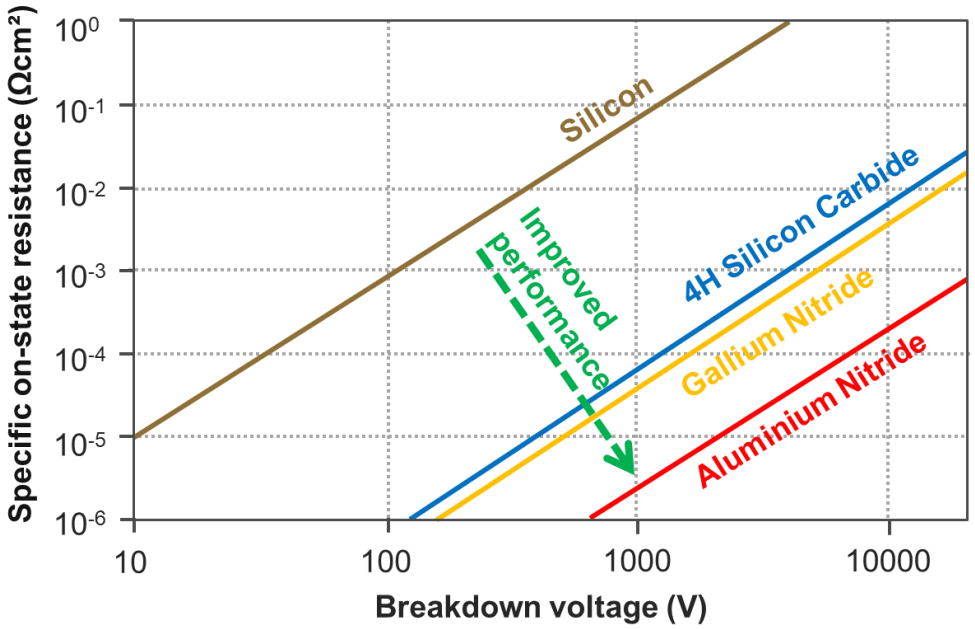


Power electronics meets microwaves



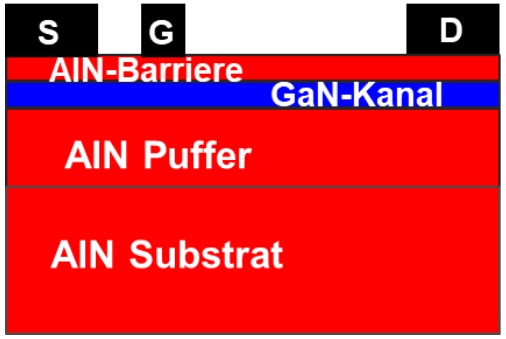
AlN-Devices: Highly efficient for power and mm-wave electronics

	Si	SiC	GaN	AlN
E_g (eV)	1.1	3.0	3.4	**6.2**
V_{br} (MV/cm)	0.3	2.4	3.3	**> 5**
λ (W/cmK)	1.5	4.5	3.2	**3.4**



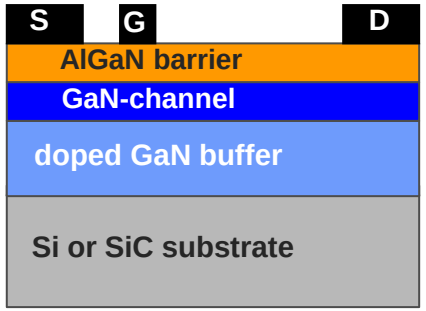
AlN-devices:

- Compact design
- High thermal conductivity
- High current density
- Highly insulating buffer
- Potentially low dispersion??
- Monolithic integration

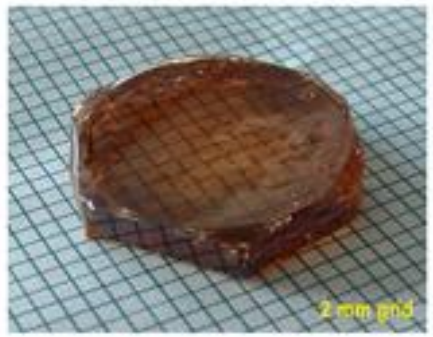


Lateral AlN/GaN/AlN HFET

FBH project „LeitBAN“ (German ministry of science and technology)

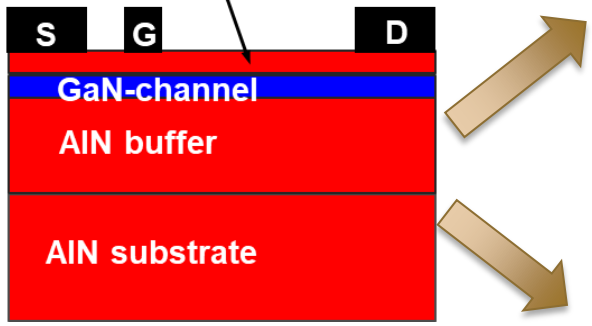


Hetero epitaxy
Defect density ~ 10^8-10^9/cm³

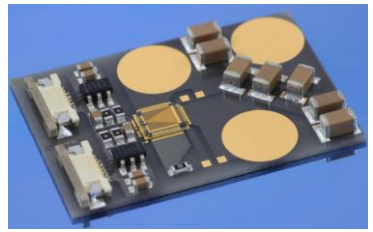


AlN crystal manufactured at Fraunhofer IIS-B

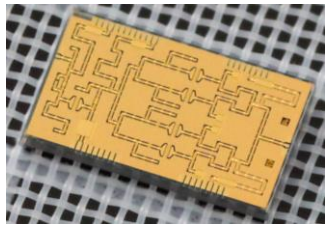
Goal



Homo epitaxy on AlN
Defect densisty ~ 10^4/cm³



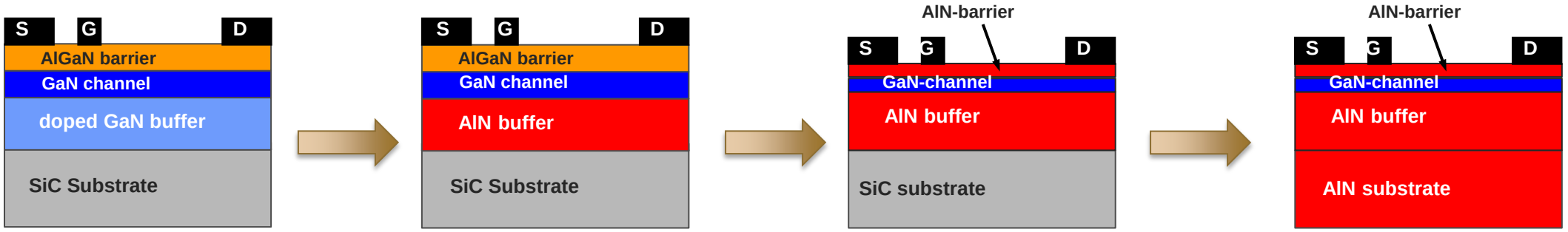
Power electronic demonstrator



mm-wave MMIC

Complete value added chain from crystal to demonstrator

Development chain



AlGaN/GaN HFET
(Hetero epitaxy)

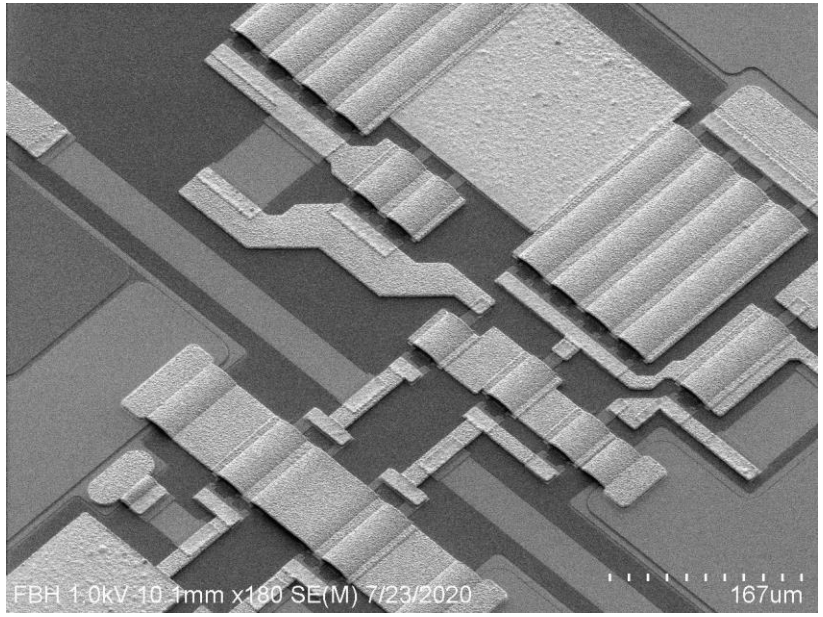
AlGaN/GaN/AlN HFET
(Hetero epitaxy)

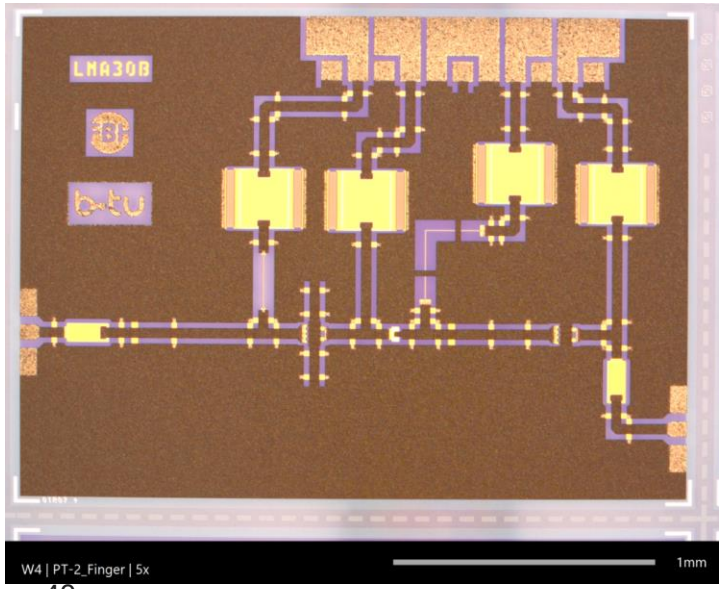
AlN/GaN/AlN HFET
(Hetero epitaxy)

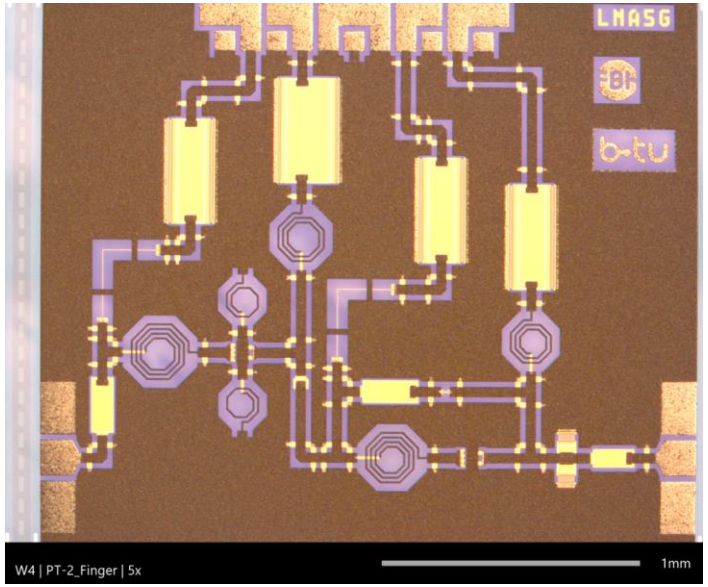
AlN/GaN/AlN HFET
(Homo epitaxy)

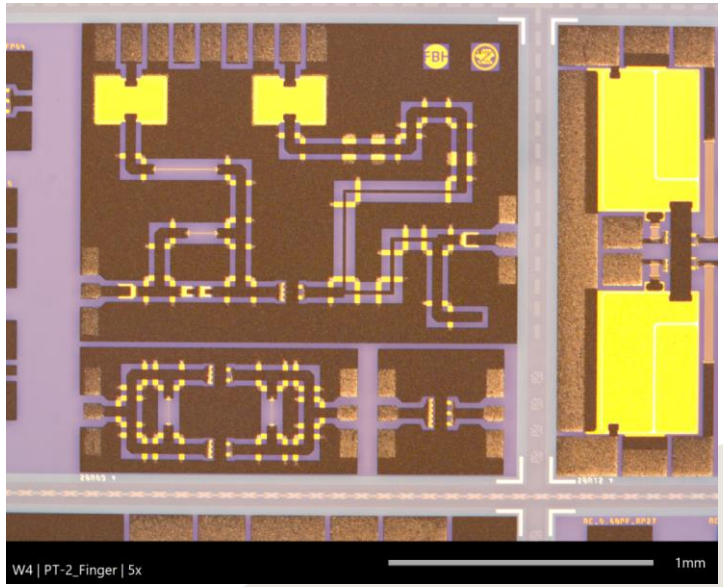
Millimeter wave devices

- 150 nm gate length
- Modelling transistors and passive structures
- Exisiting GaN power amplifier MMICs layouts
- Existing GaN low noise amplifier MMICs layouts





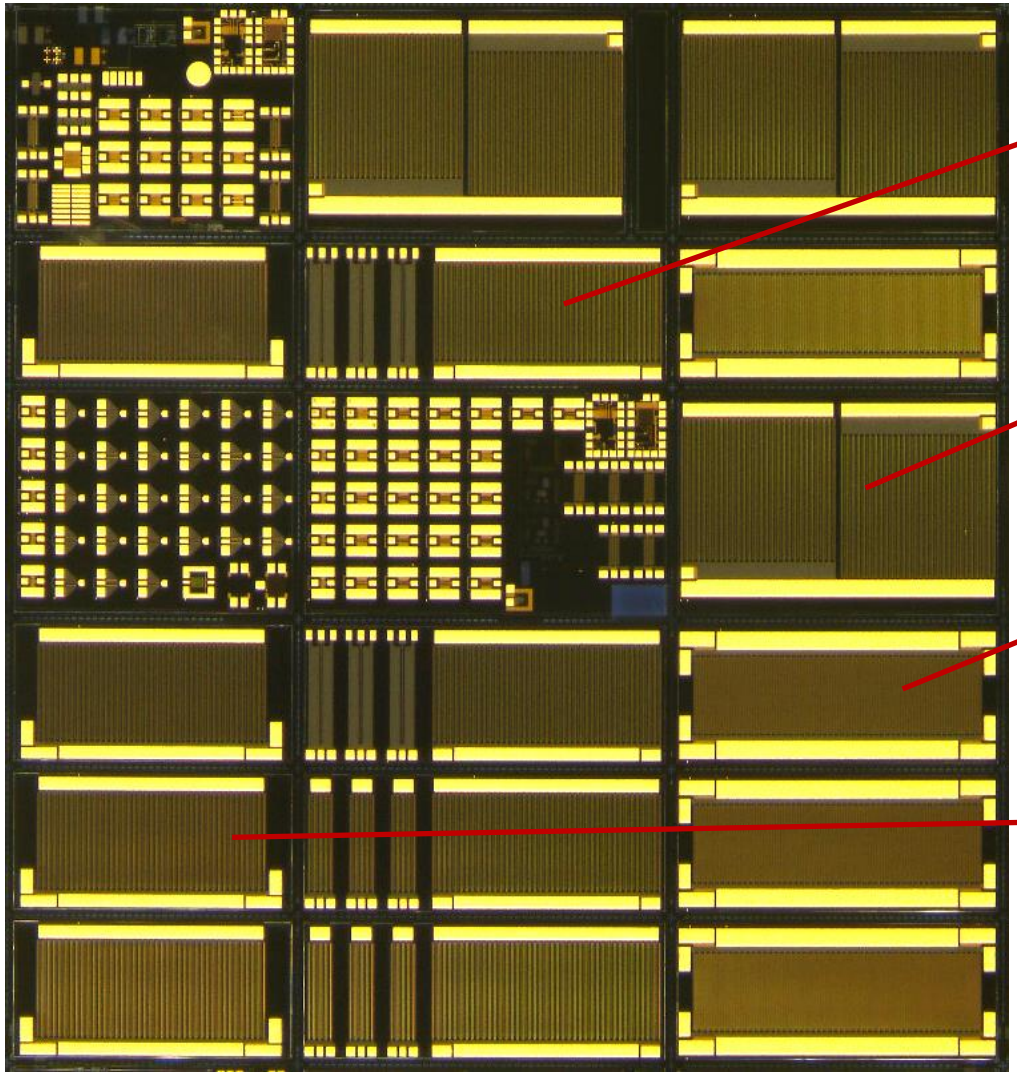




HV power devices

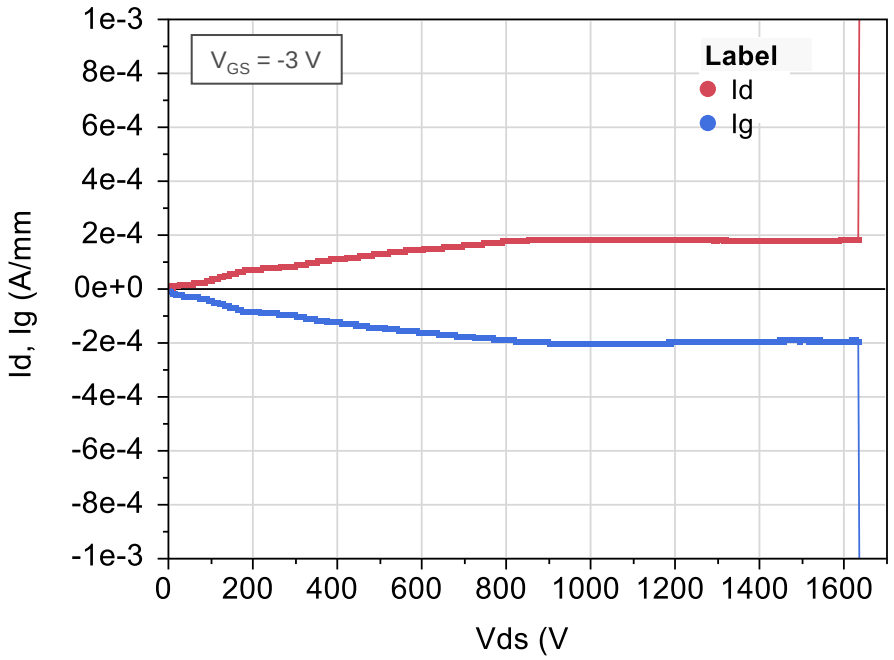
All devices

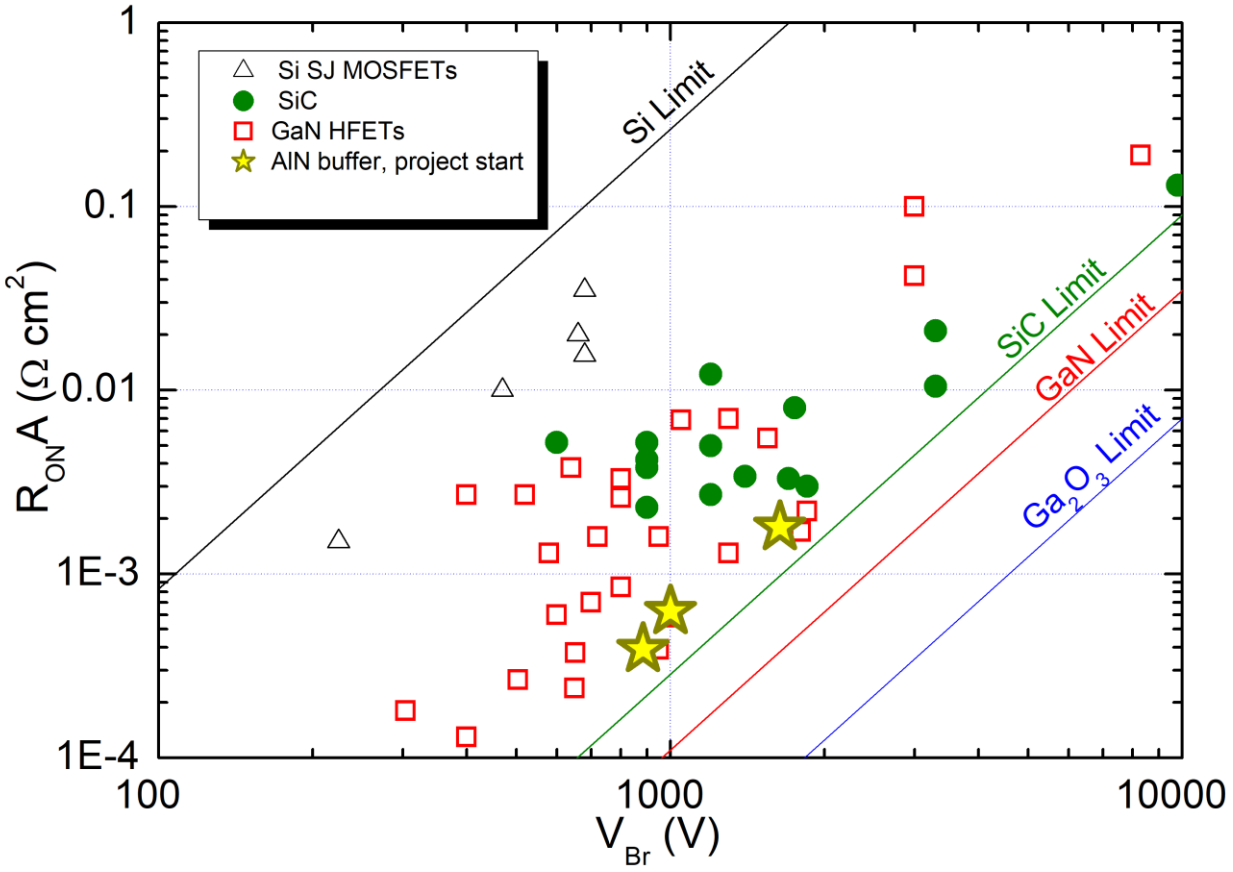
- 92 mm gate width → 150-200 mΩ devices
- 18 µm gate-drain separation → 1200 V
- No overlapping field plates (no 2nd SiN) to keep off-state leakage low
- Source connected FP version „FP7“
- New Kelvin-source pads introduced for 90° rotated bond wires between gate drive circuit and power circuit



AlN buffer power switching benchmarking 2019

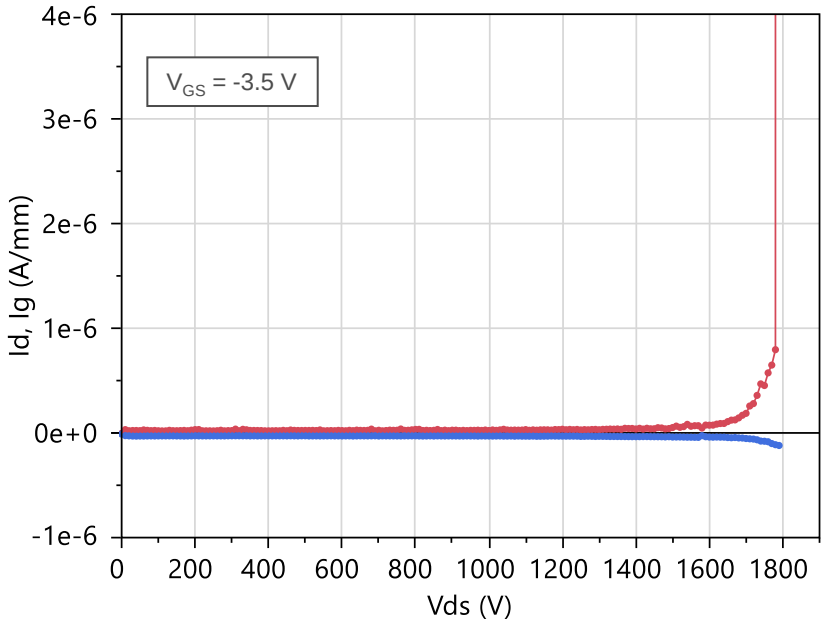
FP7, 19R12, S52, d_{GD} = 15 µm, d_{SD} = 17.2 µm
→ A = 1.72e-4 cm²
→ **V_{Br} = 1636 V**
→ R_{ON} = 10.45 Ωmm → **R_{ON}xA = 1.797e-3 Ωcm²**

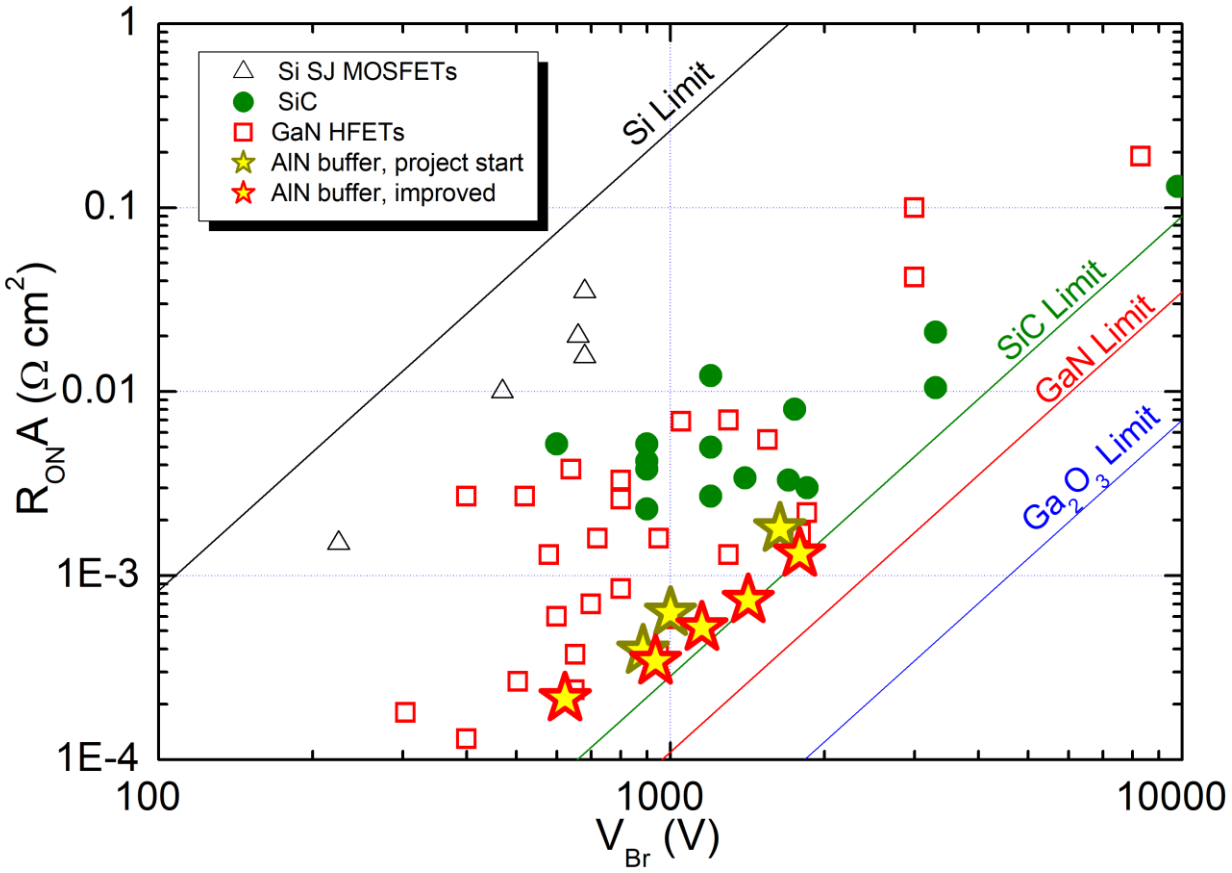




AlN buffer power switching benchmarking 2020

HS_L2, 21R02, S42, d_{GD} = 15.2 µm, d_{SD} = 17.2 µm
→ A = 1.72e-4 cm^2
→ **V_{Br} = 1790 V**
→ R_{ON} = 7.6 Ωmm → **R_{ON}xA = 1.315e-3 Ωcm²**



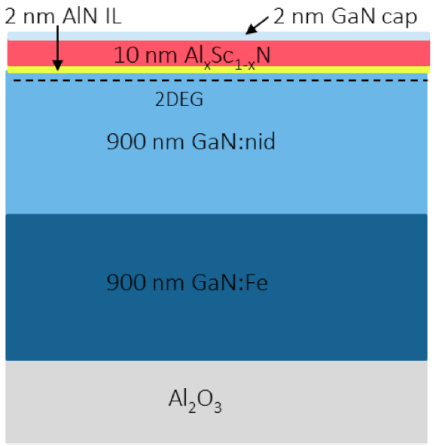


- Improved AlN buffer quality gives higher V_{Br}
- Thicker GaN channel gives lower R_{ON}

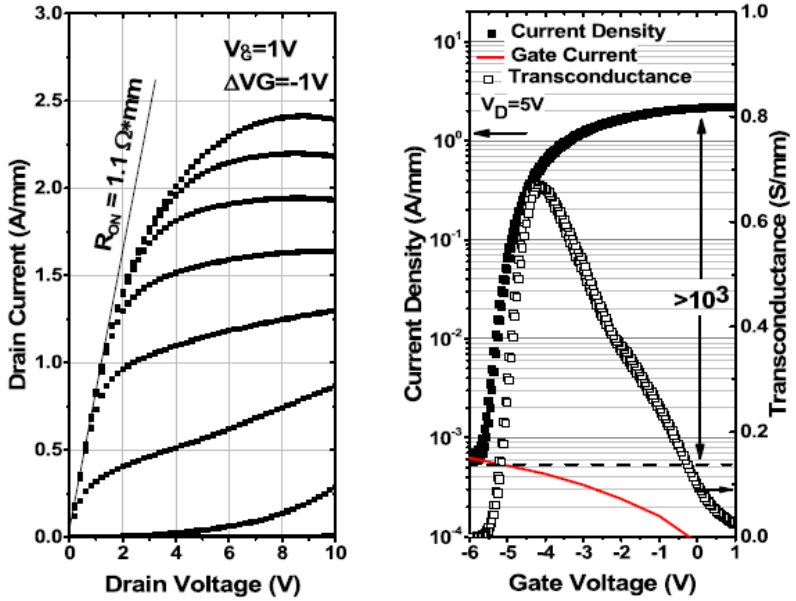
AlScN devices

Advantages:

- High spontaneous polarization difference to GaN
  → high 2 DEG electron density
  → up to 2.4 A/mm current density
- MOVPE growth possible
- Lattice matched to GaN with $Al_{0.82}Sc_{0.18}N$ combination
- Technology still has to be developed



S. Leone: J. Appl. Phys. 127, 195704 (2020); doi: 10.1063/5.0003095



Green et al.: IEEE Electron Device Letters, Vol. 40, no. 7, July 2019

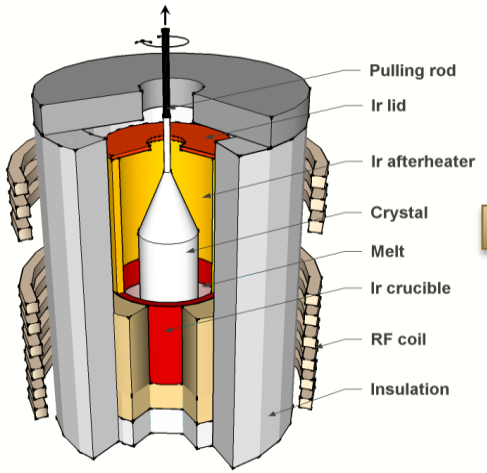
β-Ga_2O_3: Comparison to other semiconductor devices

	Si	GaAs	4H-SiC	GaN	β-Ga_2O_3
Band gap energy E_g (eV)	1.1	1.4	3.26	3.4	4.6-4.9
Electric breakdown field E_{crit} (10^6 V/cm)	0.3	0.4	2.2	3.3	8 (est.)
Relative dielectric constant ε_r	11.9	12.9	10.1	9	10
Thermal conductivity k (W/Kcm)	1.5	0.55	4.5	2.3	0.23 in [010] dir. 0.13 in [100]
Bulk electron mobility μ_e (cm^2/Vs)	1350	8000	900	1200	300
Saturation velocity v_{sat} (10^7 cm/s)	1.0	2.0	2.0	3	not published in detail
Baliga´s FOM related to Si ($\varepsilon_r \mu_e E_{crit}^3$)	1	15	340	870	3444

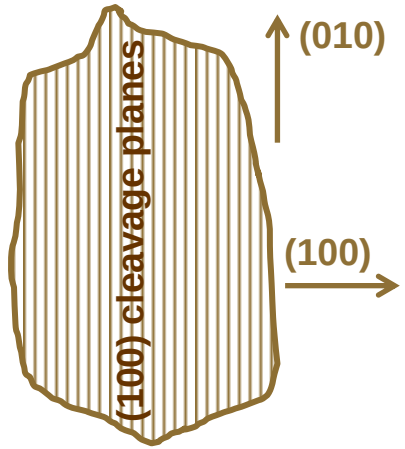
M. Higashiwaki et al: Appl. Phys. Lett., 100, 013504, (2012)

Ga_2O_3 device development chain. Wafering and epitaxy

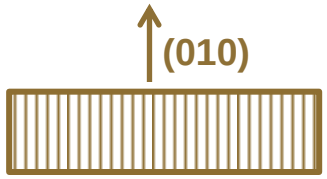
Ga_2O_3 growth Czochralski method



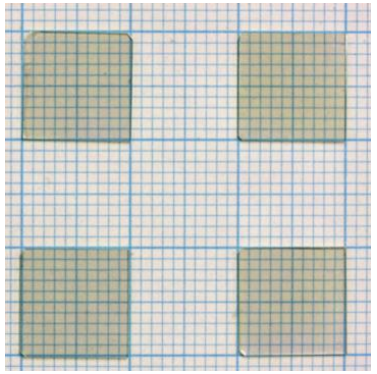
Semi-insulating Mg-doped Ga_2O_3 crystal (2”)



Ga_2O_3 slab, 1 cm thick cut out from boule



Ga_2O_3 wafer cut out from slab (1x1 cm²)



Device process

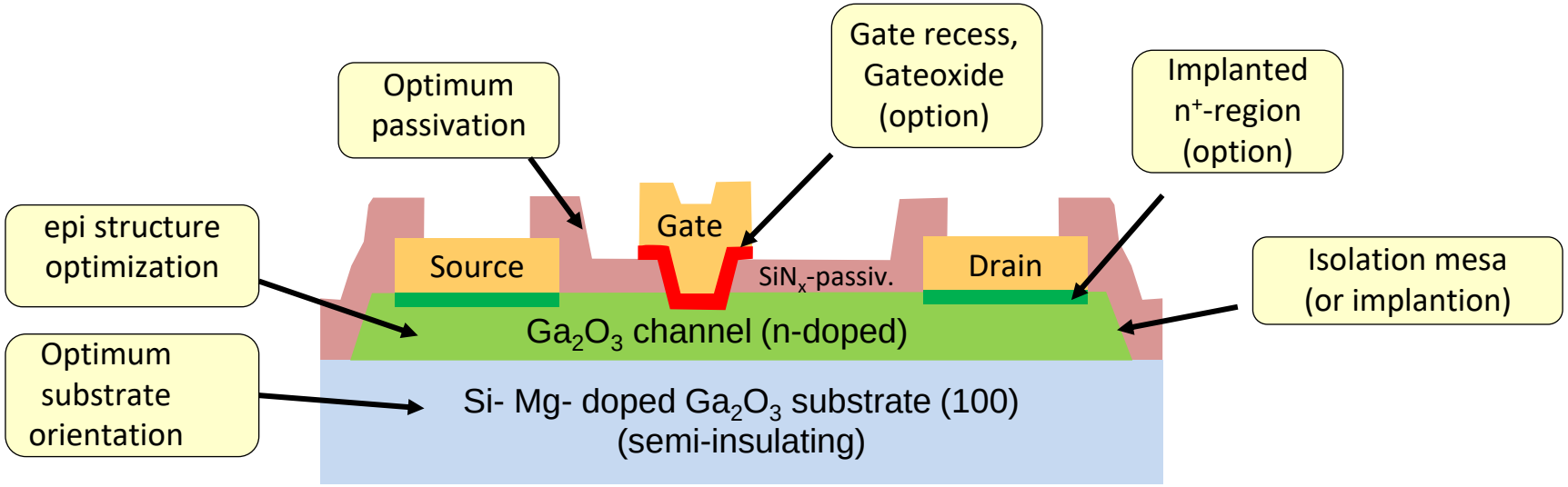
Lattice orientation	λ (W/(cmK))
(100)	10.9
(001)	21
(010)	29

Leibniz-Institut für Kristallzüchtung (IKZ)

M. Baldini et al., J. Mat Sci in Semicond. Processing 2018

Leibniz Ferdinand Braun Institut

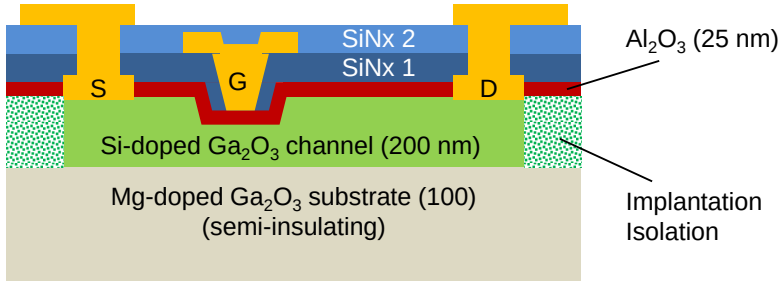
Process and epi optimization

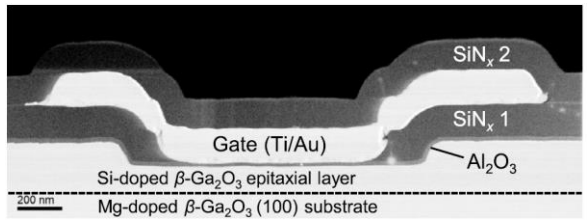


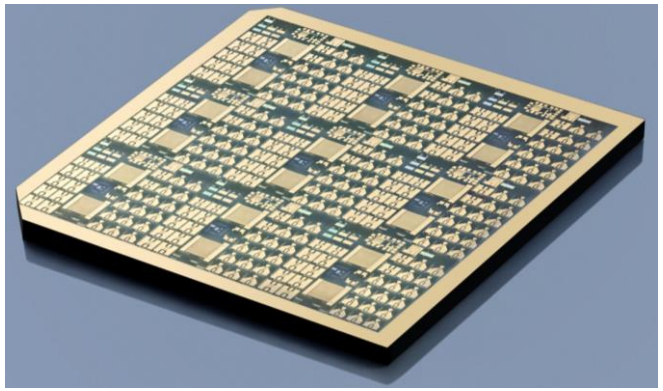
Critical technological steps

- Epitaxy: Properties strongly depend on device orientation (anisotropy of electron mobility and thermal conductivity
- Processing
  - Lithography on small wafers (1x1cm²)
  - Gate oxide technology in conjunction with gate recess (ALD Al_2O_3)
  - Ohmic contacts (n^+ - doping using Ge^+ -Implantation)
  - Device isolation (N^+ -Implantation)

Example of lateral device technology (1): Substrate, epi and processing







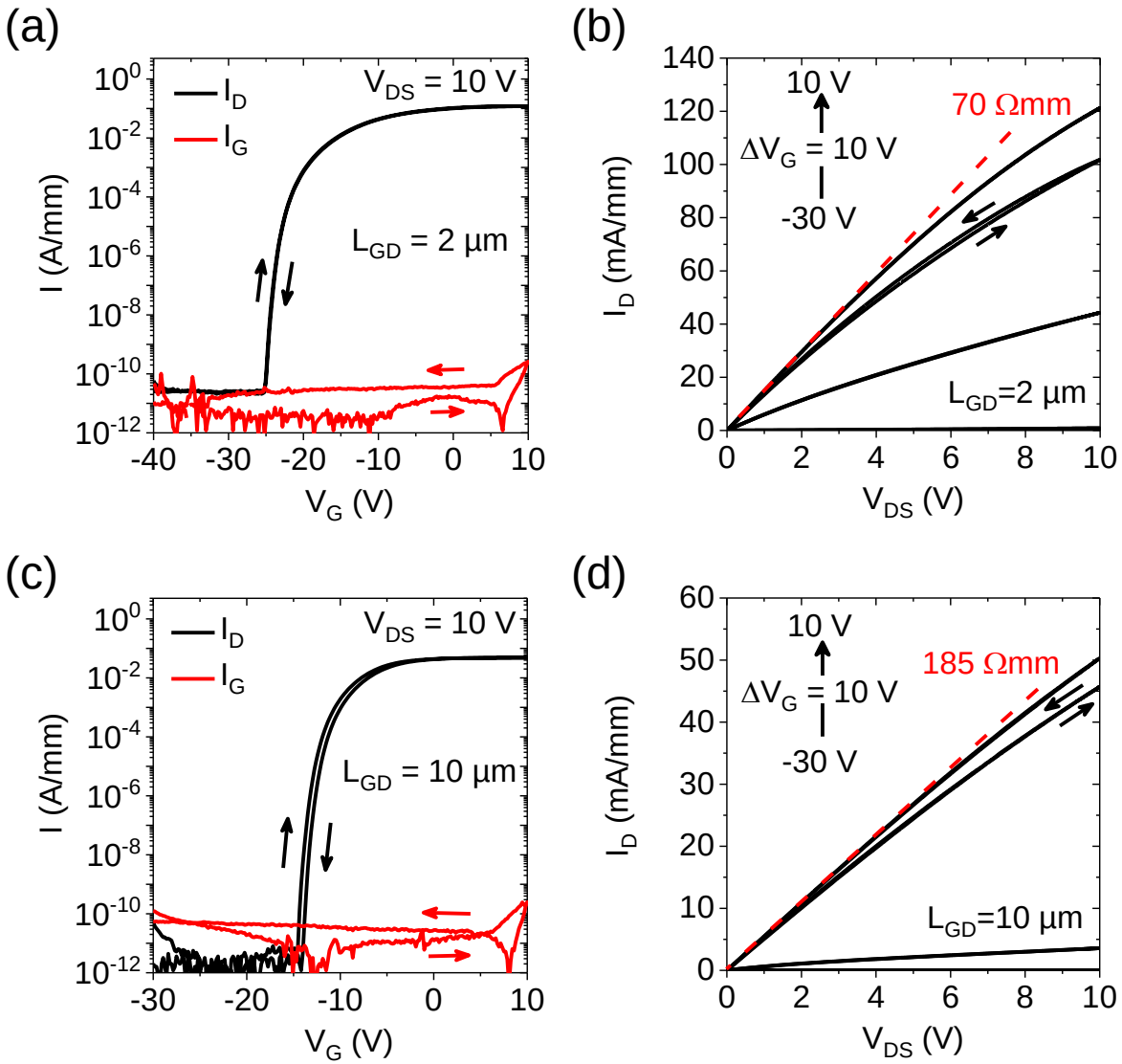
Substrates

- 1x1 cm² Ga_2O_3 Mg compensated substrate
- Special technological approach for wafer stepper lithography

Processing sequence:

- Gate recess etching
- AlD Al_2O_3 gate insulator deposition
- SiN_x deposition (1st passivation)
- Isolation implantation
- Gate trench etching (gate length 0.7 µm)
- Gate metal deposition (TiAu)
- SiNx deposition (2nd passivation)
- Opening of contact windows
- Interconnect metal deposition

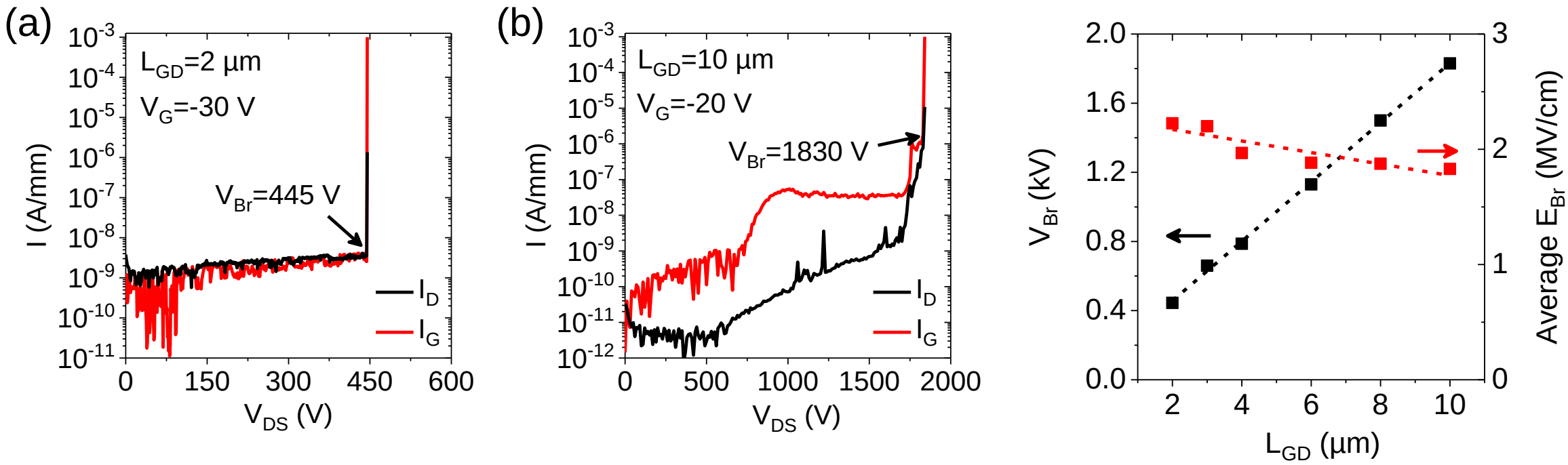
Example of lateral device technology (2): DC device results



- Extremely low leakage
  - Gate leakage < = 10^{-11} A/mm
  - Drain leakage < 10^{-10} A/mm
- On-off ratio > 10^8
- Negligible hysteresis of MIS gate
- Drain current > 120 mA/mm
- On-state resistance 70 Ωmm → 185 Ωmm as LGD increases from 2 to 10 µm

IEEE Electron Device Letters, Vol. 40, No. 9, September 2019

Example of lateral device technology (3): Device breakdown

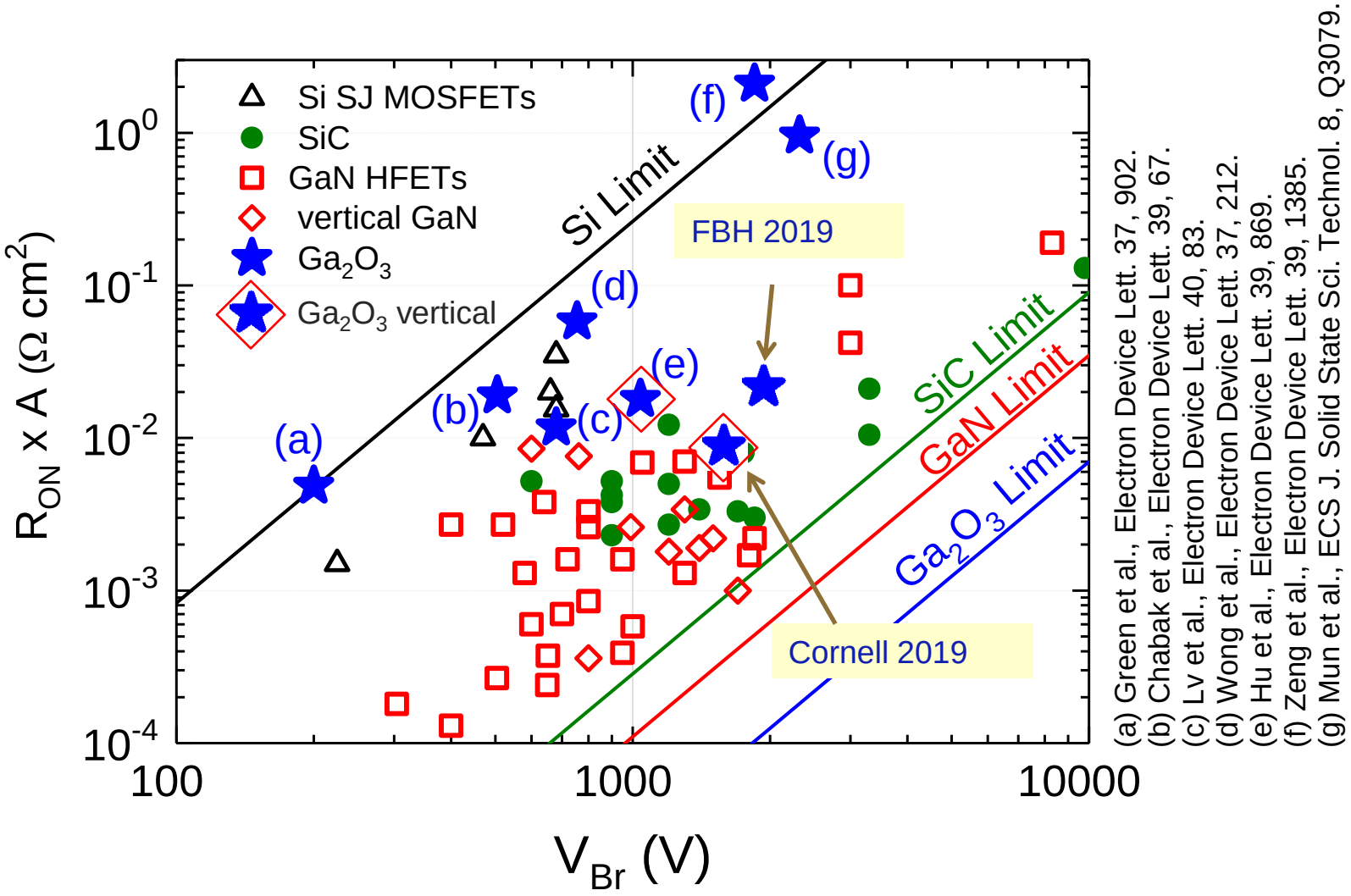


- Breakdown linearly scales with gate / drain distance
- Breakdown field around 200 MV/cm

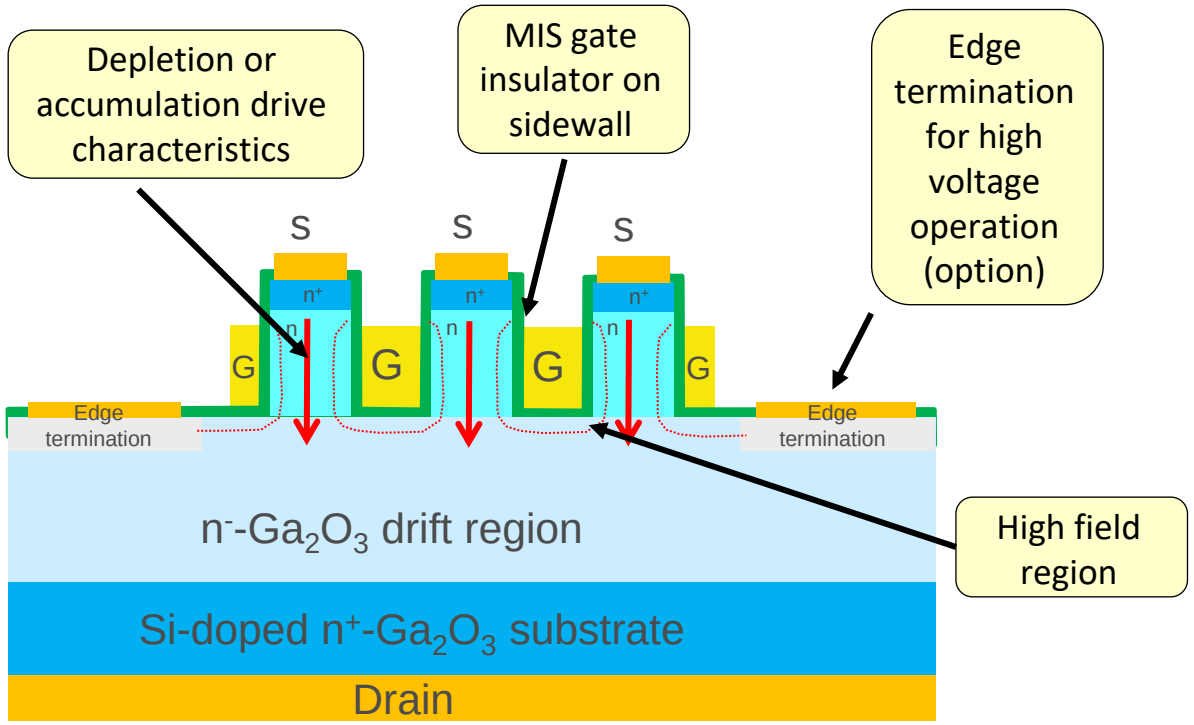
Very good trade-off between breakdown voltage and on state-behaviour

IEEE Electron Device Letters, Vol. 40, No. 9, September 2019

State-of-the-art and comparison to other device families

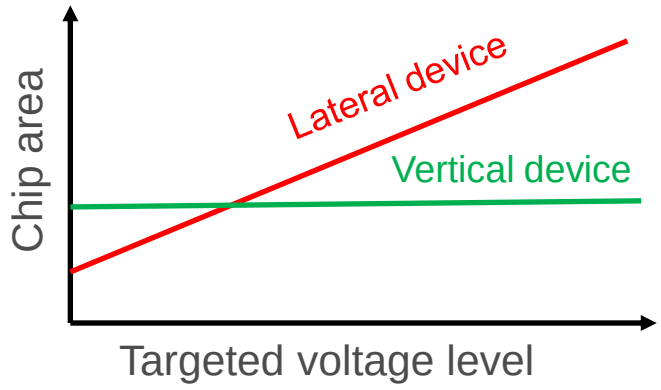


Vertical devices

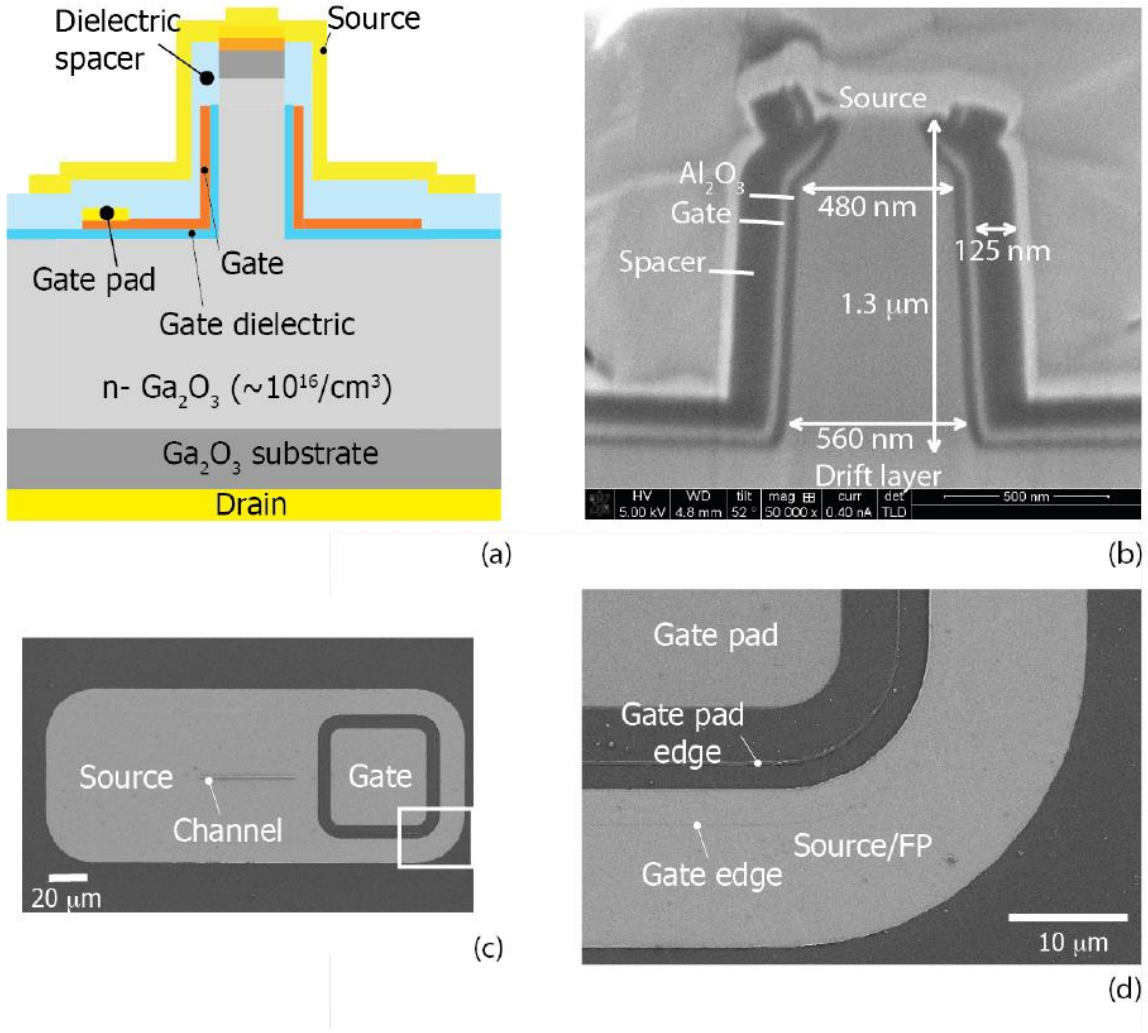


Depletion or accumulation type device

- Significant advantages:
  - Voltage drop over epitaxial layer if device is turned off – ideal separation of high potentials
  - Requires lower chip area at high voltage levels
- Disadvantages
  - Controlled n^--doping for drift zone less than $1x10^{16}$ / cm^3 depending on targeted voltage level
  - Requires new concepts for edge termination and control of high-field region at trench bottom sidewall



Example of vertical device technology (2): processed FinFET

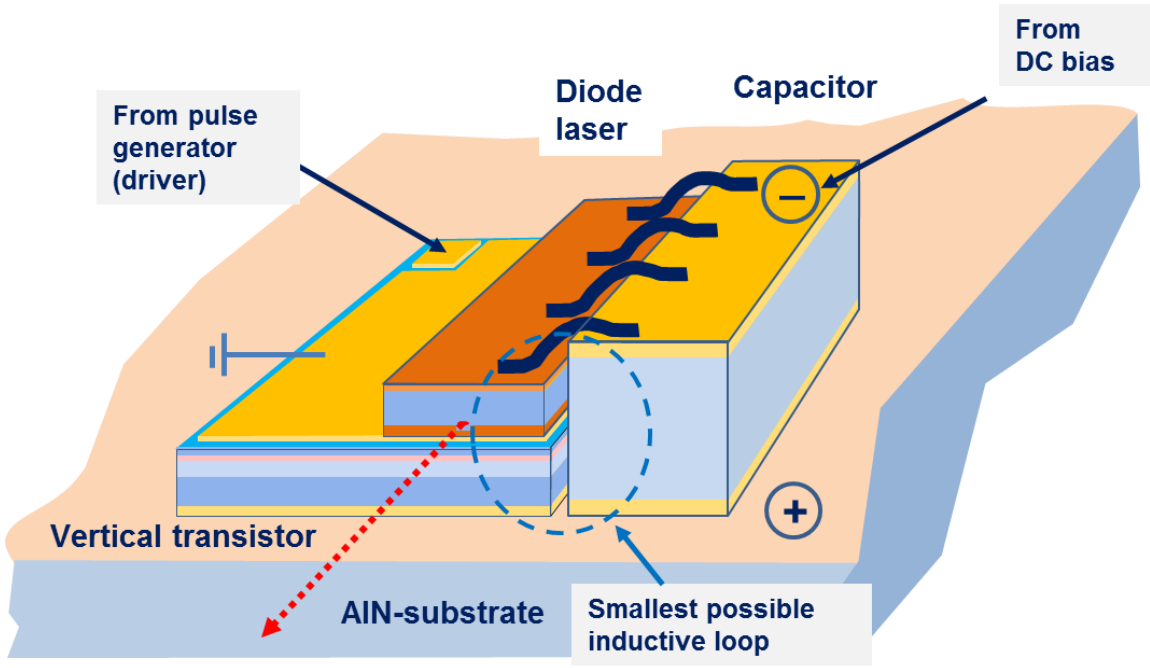


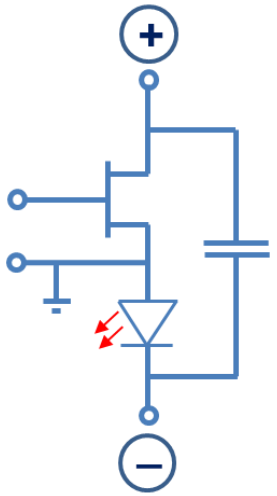
High voltage engineering

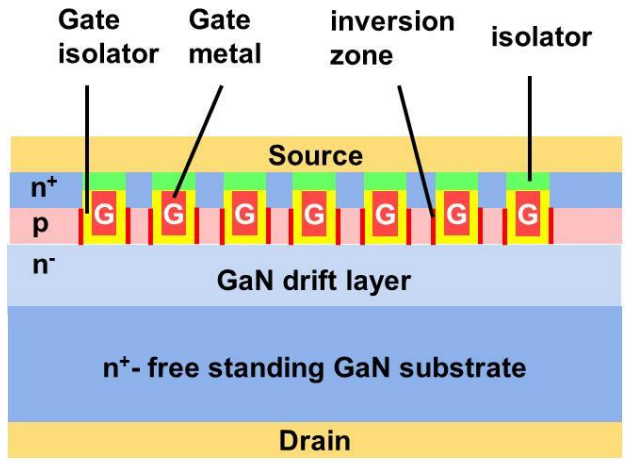
- Field plates tom suppress critical field regions (backed with FE simulations)
- Optimized layout for high voltage
  - Rounded structures to avoid E-field crowding

Taken from: Proceedings of the 31st International Symposium on Power Semiconductor Devices & ICs
May 19-23, 2019, Shanghai, China

GaN verticval trench MISFETs for direct laser driving

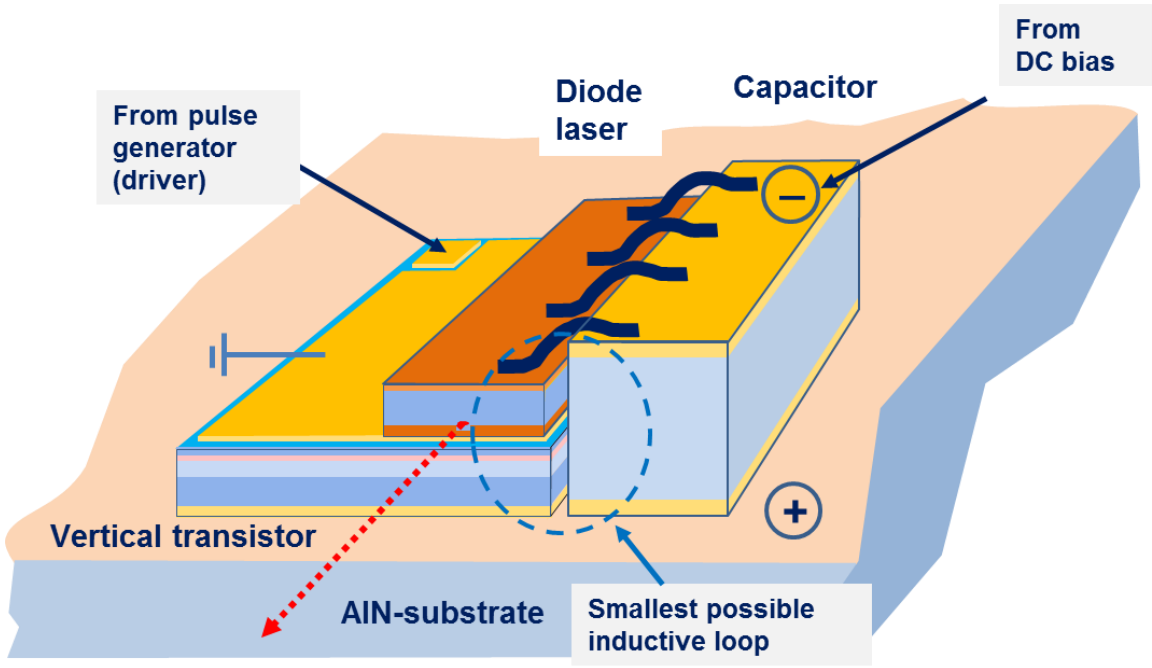


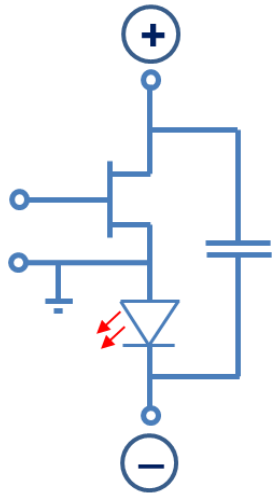




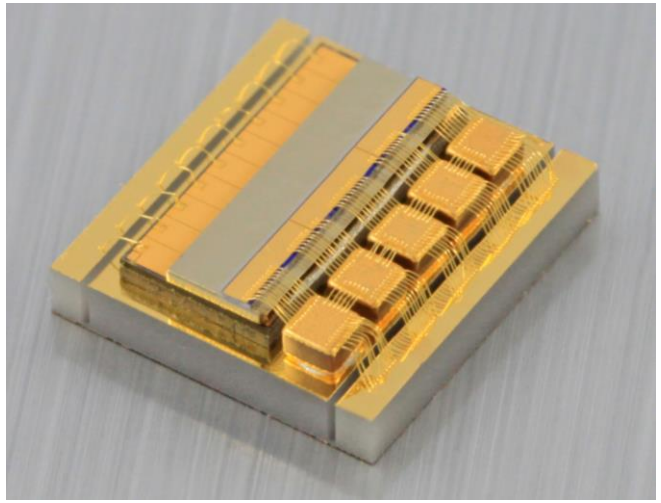
- Idea: Reduce parasitic inductances by developing an ultrafast “electronic valve“
- Chip-on-chip hetero integration
- Requires “true vertical” GaN devices

Test of mounting schemes for heterointegration





Heterointegration of laser, GaN transistor and capacitors on AlN submount (~ 7x7 mm²)

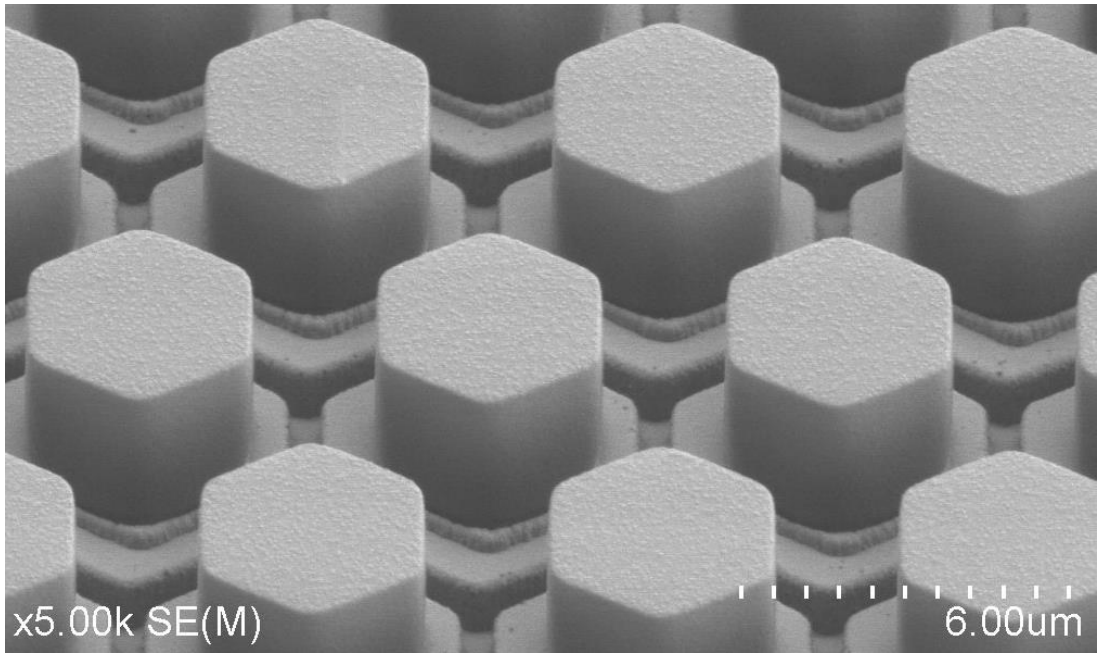


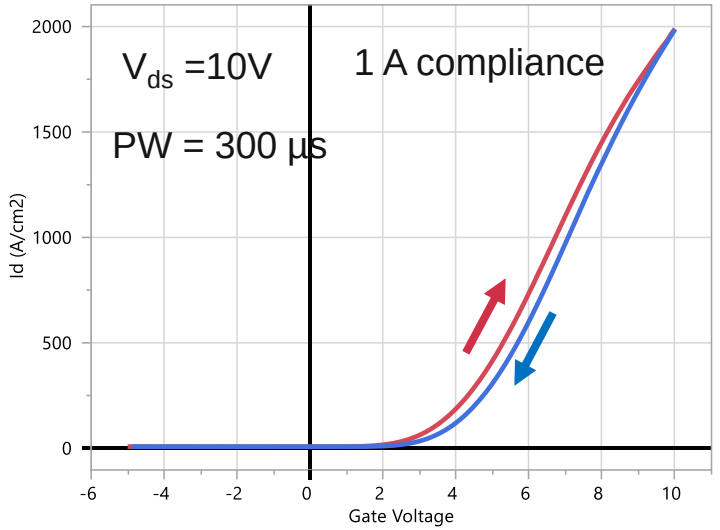
- Laser – GaN switch heterointegration
  - High-speed core with integrated capacitors
  - Mounted on AlN interposer

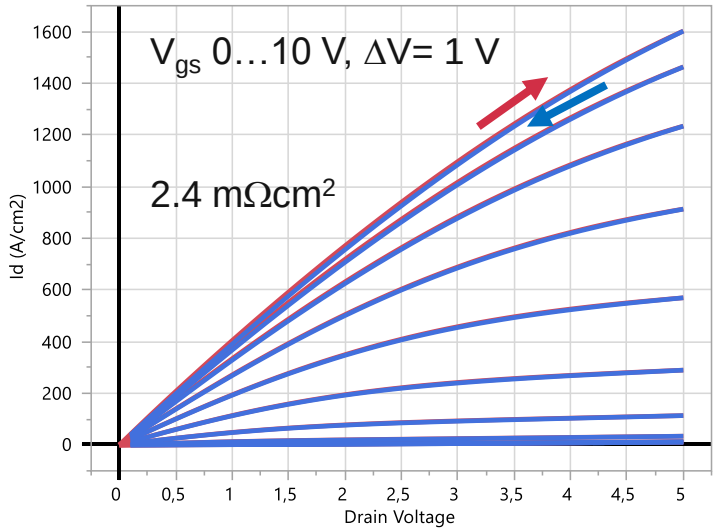
Impressive results obtained

- Scaling concept works
  → Current density of up to 4000 A/cm² obtained with moderate scaling concepts

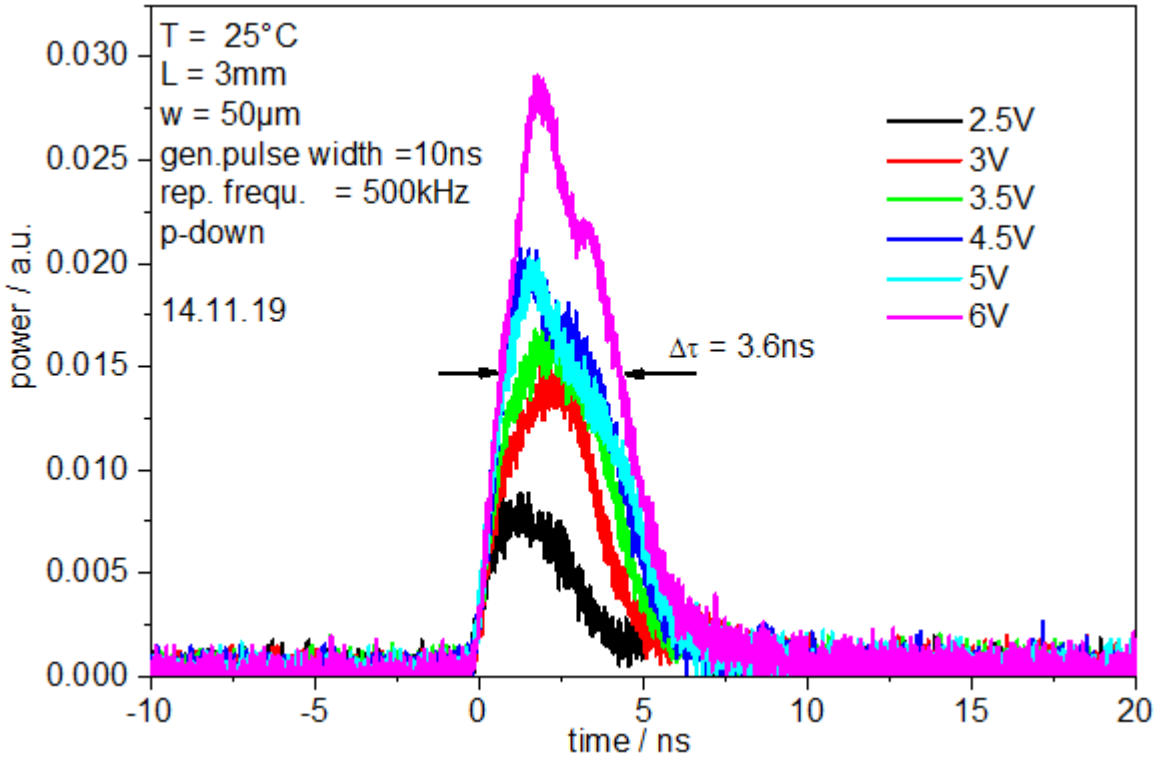
- Nearly hysteresis free devices
  → gate technology development made good progress



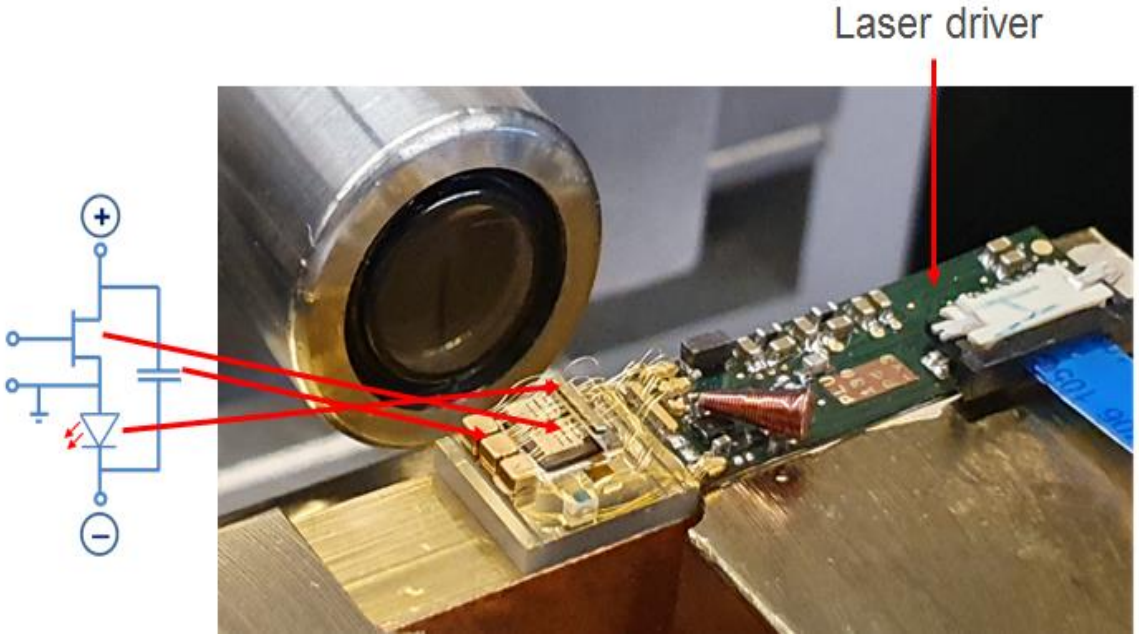




Cip-on-chip mouinting vertical GaN – diode laser



GaAs based DBR-BA laser 903 nm



3.6 ns pulses, about 5 W optical power

Conclusions

GaN power switching devices reached high maturity – world wide

- Optimum device switching at high voltage is still an quality characteristics
  → it is very different for different device vendors
- New material schemes are coming up: AlN, AlScN….

High switching speed of GaN power devices has been demonstrated

- Monolithic and hybrid integration techniques necessary to further increase speed
- However: Monolithic integration of half bridges still a problem especially for high voltage applications

Future developments

- Hybride and monolithic integration schemes → think in terms of high frequency
- High voltage vertical GaN devices
- Gallium oxide lateral and vertical devices