MICROELECTRONICS FOR BRAIN MACHINE INTERFACE

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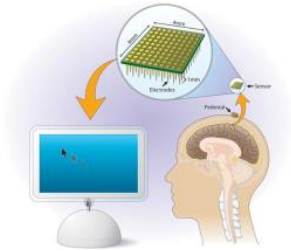
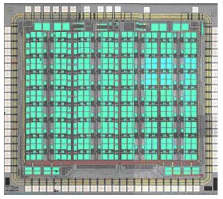
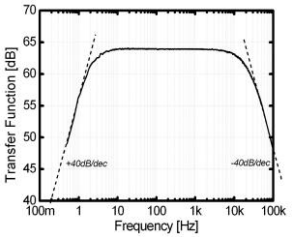
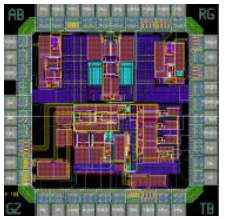
Outline

- The Brain Machine Interface concept
- Front-end amplifier design
- Experimental results
- Ongoing projects
- Conclusions



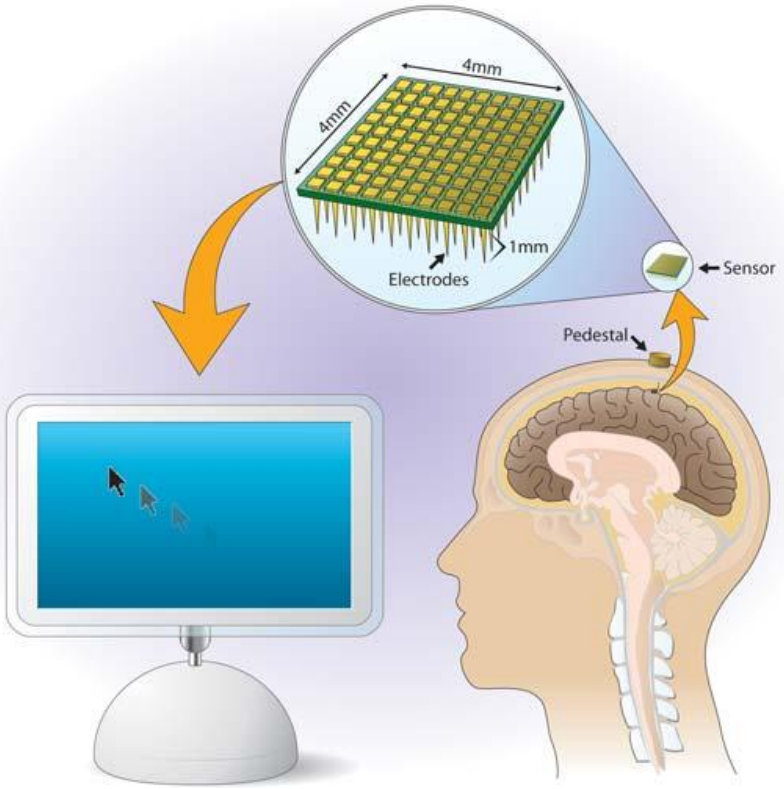




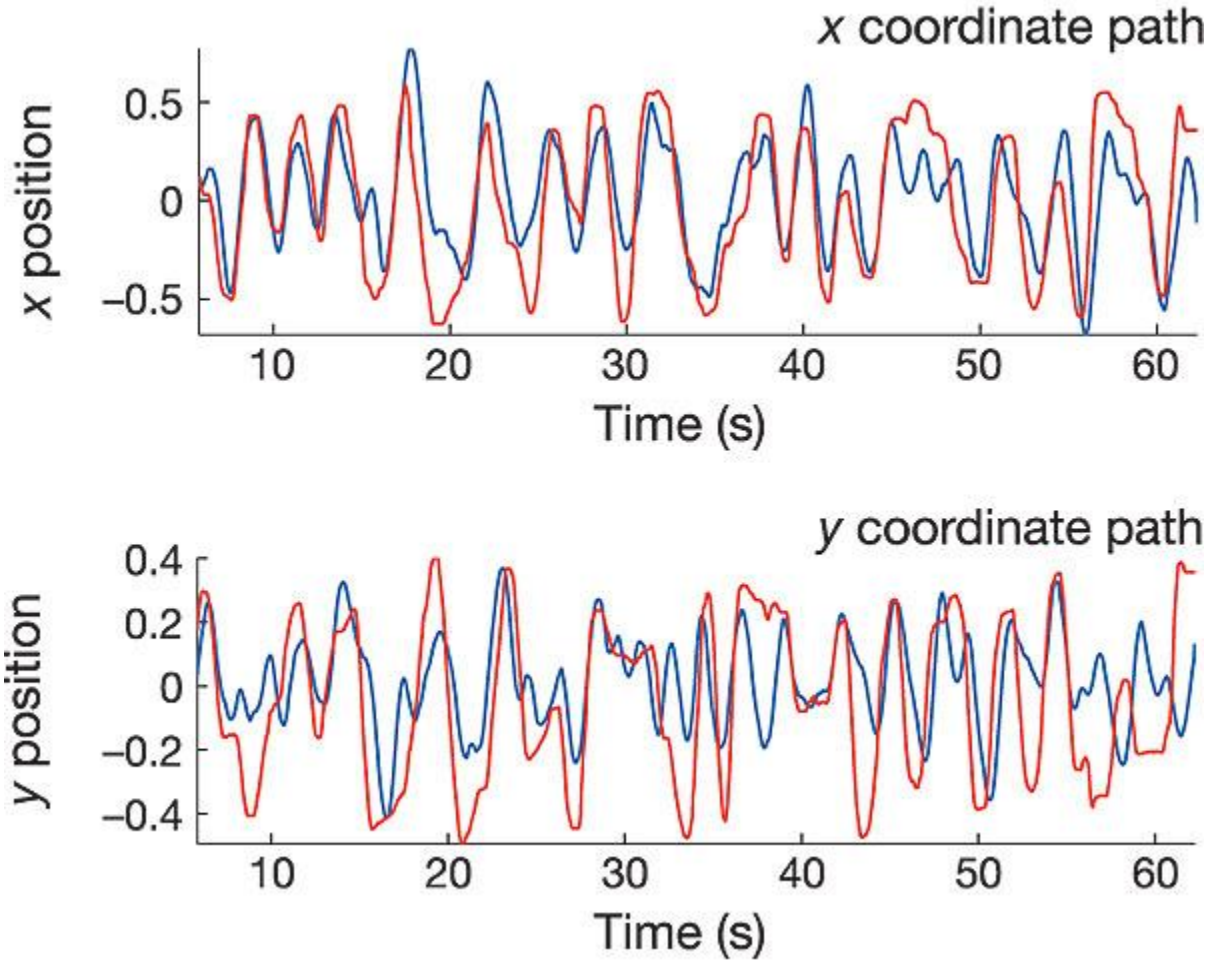


Brain Machine Interface (BMI)

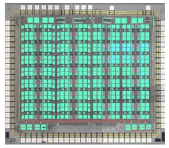
The BMI concept



Proof of concept



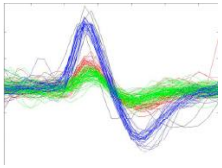
The goal



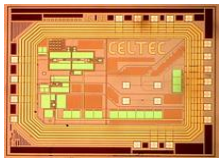
The project goal is to shrink bulky instruments into implantable integrated circuits

The BMI electronics

Robotic arm



Processing

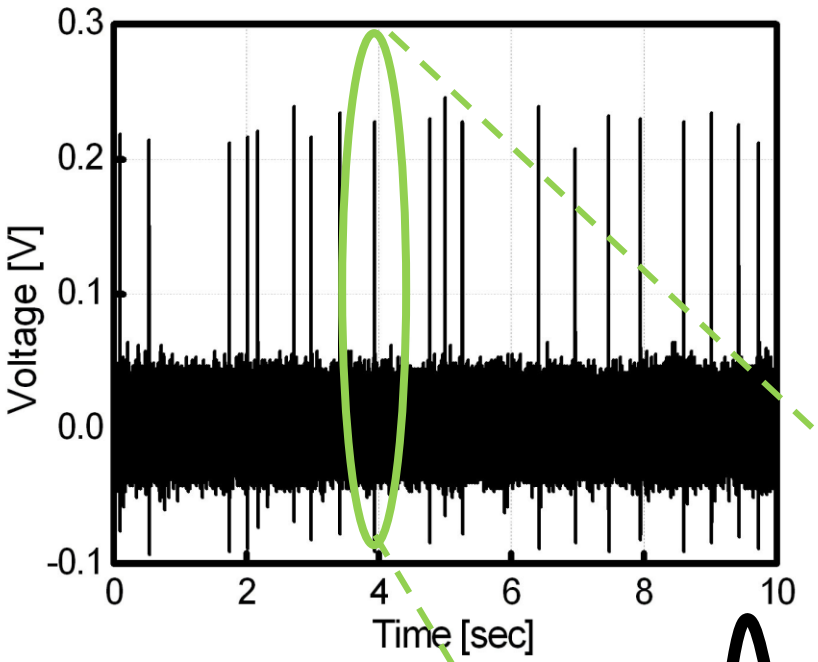


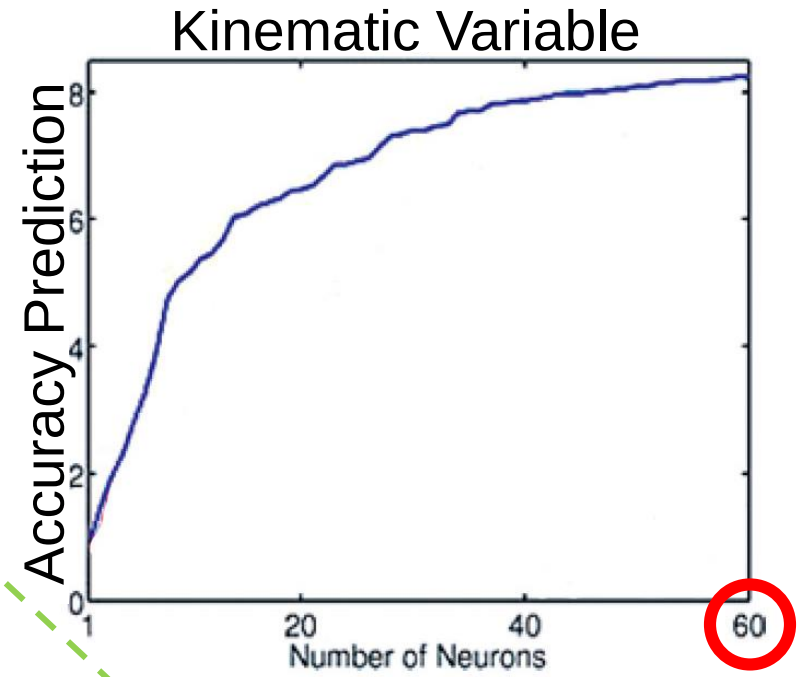
Signal readout

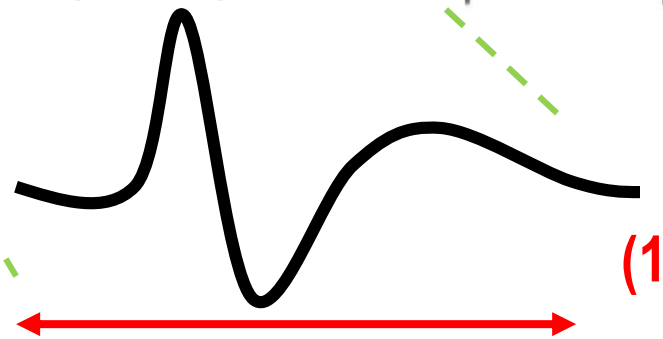
Multi Electrodes

Brain

Neural signal







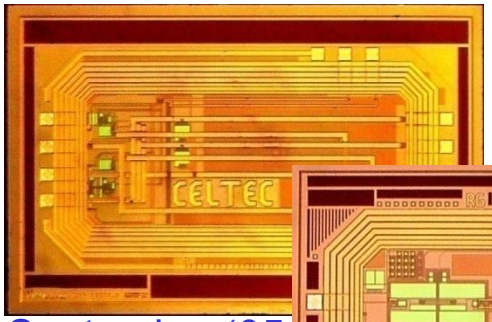
~10-100 µV

~1ms
(100 Hz – 10 kHz Band)

Amplifier requirements

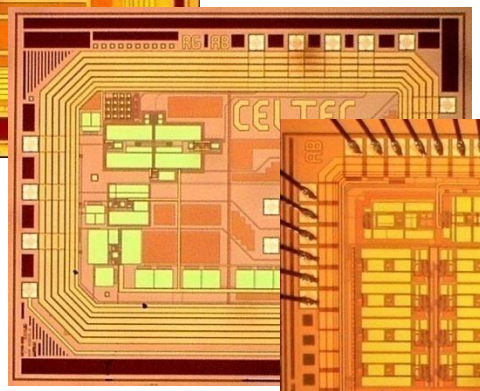
- Low-noise amplifier (< 5 μV_{rms})
- Low-power (to prevent tissue damage)
- Eliminate electrode-tissue DC offset (~100 mV)
- Deliver > 60 dB gain for a signal bandwidth of 10 kHz
- High Input Impedance (> 10 MΩ @ 1kHz)

Design history



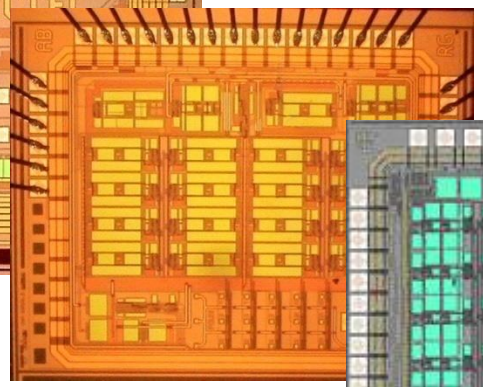
1 channel

September ‘05



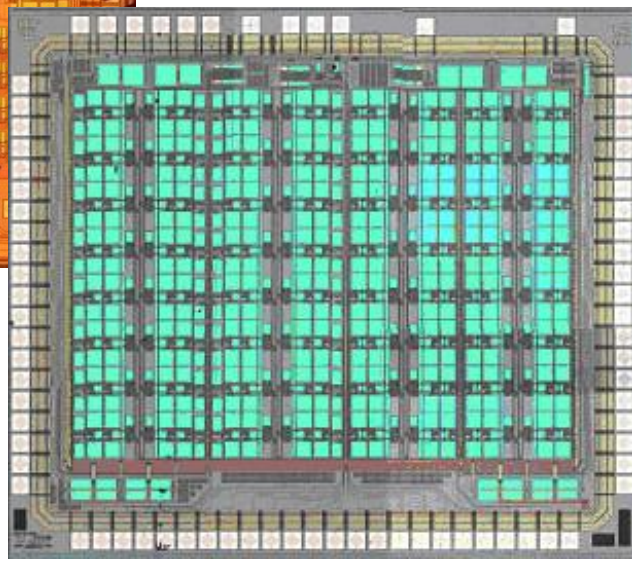
4 channels

February ‘06



16 channels

December ‘06

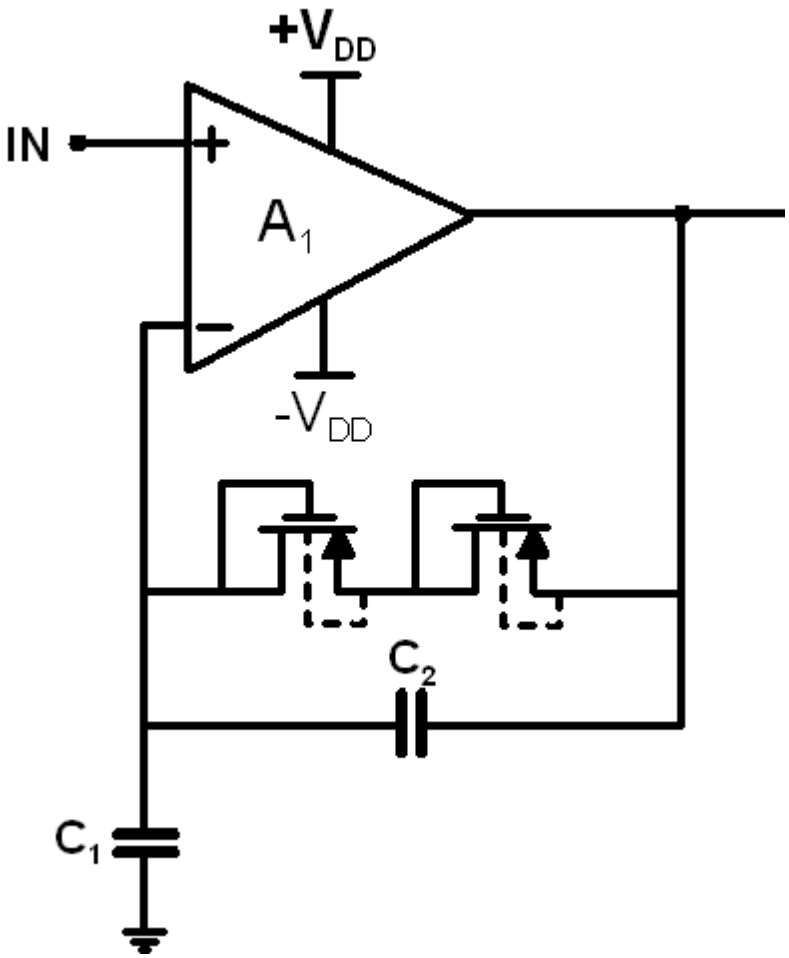


64 channels

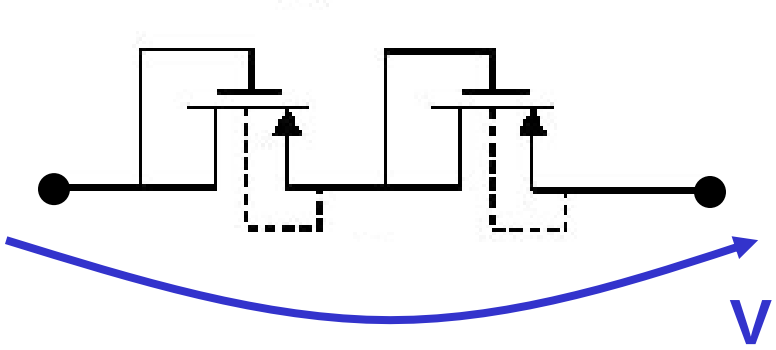
March ‘07

Front-end Design

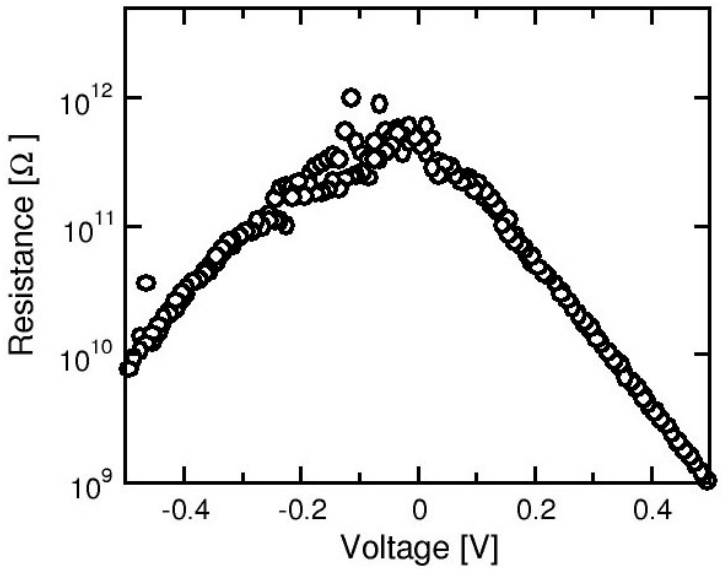
Front-end



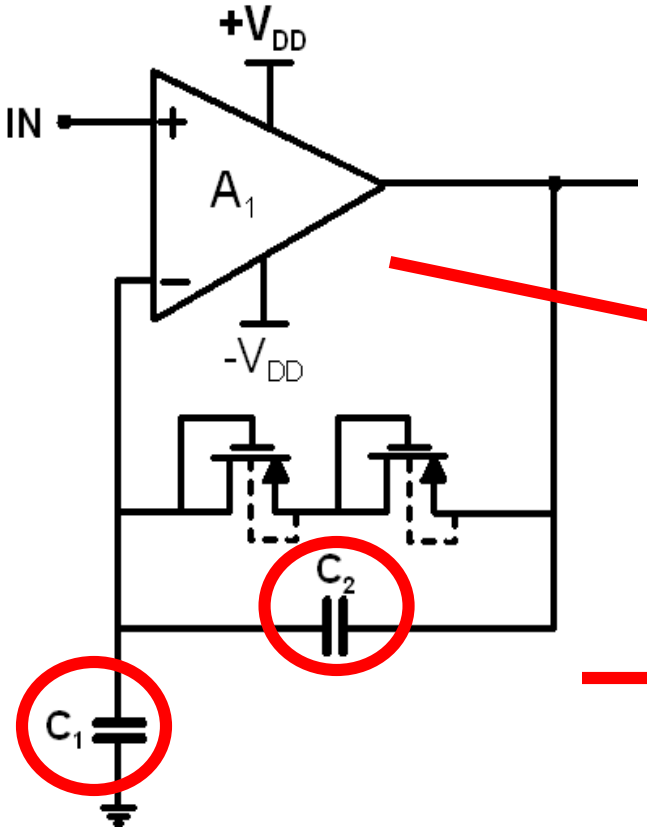
Feedback element



MOS devices used as high-value resistors (Harrison, 2003)



Gain



Band-pass Filter

Low-pass pole:

– $GBWP/G_1 \sim 20$ kHz

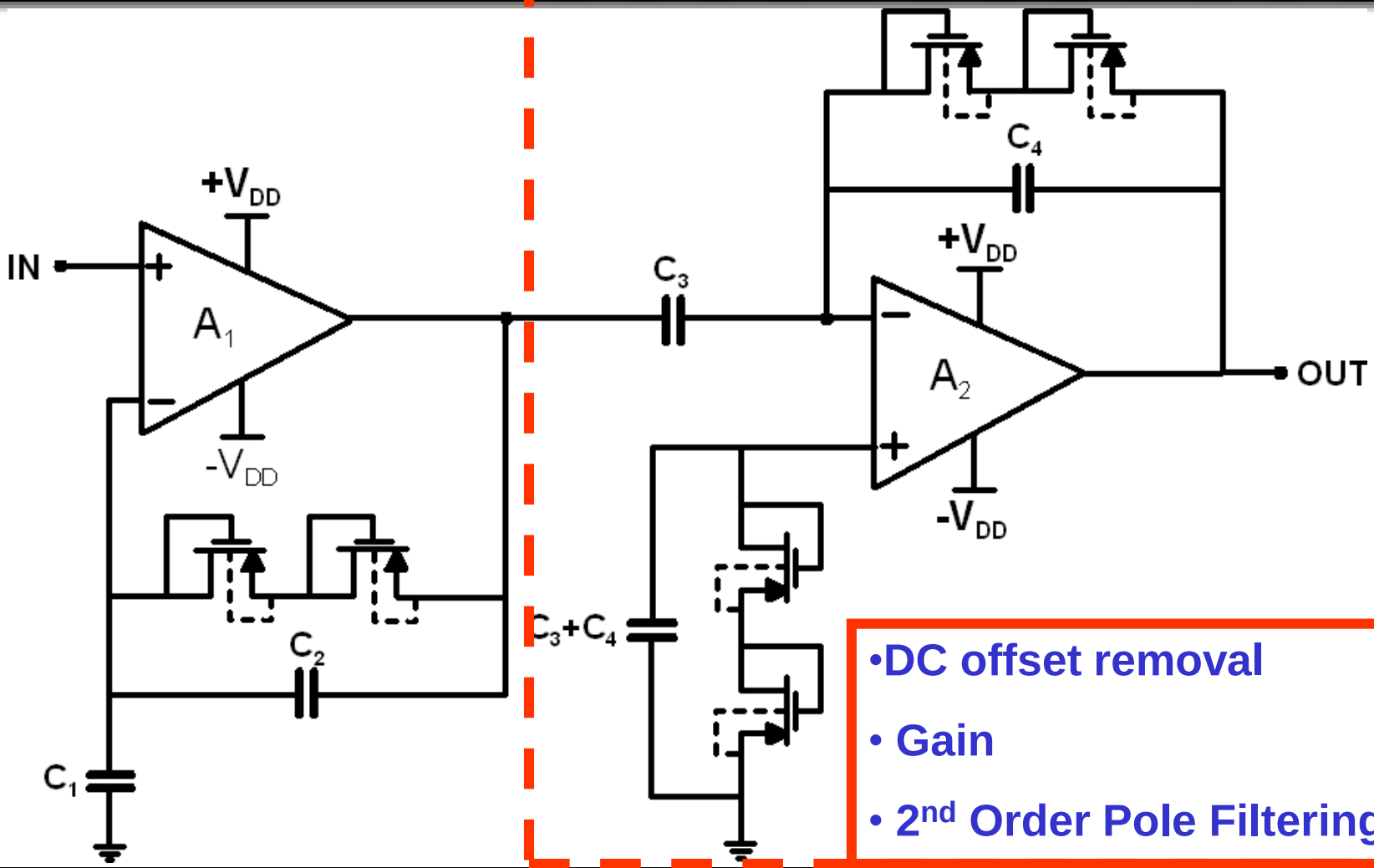
Midband Gain

$G_1 = (C_1+C_2)/C_2 \sim 50$

$C_1 = 10$ pF

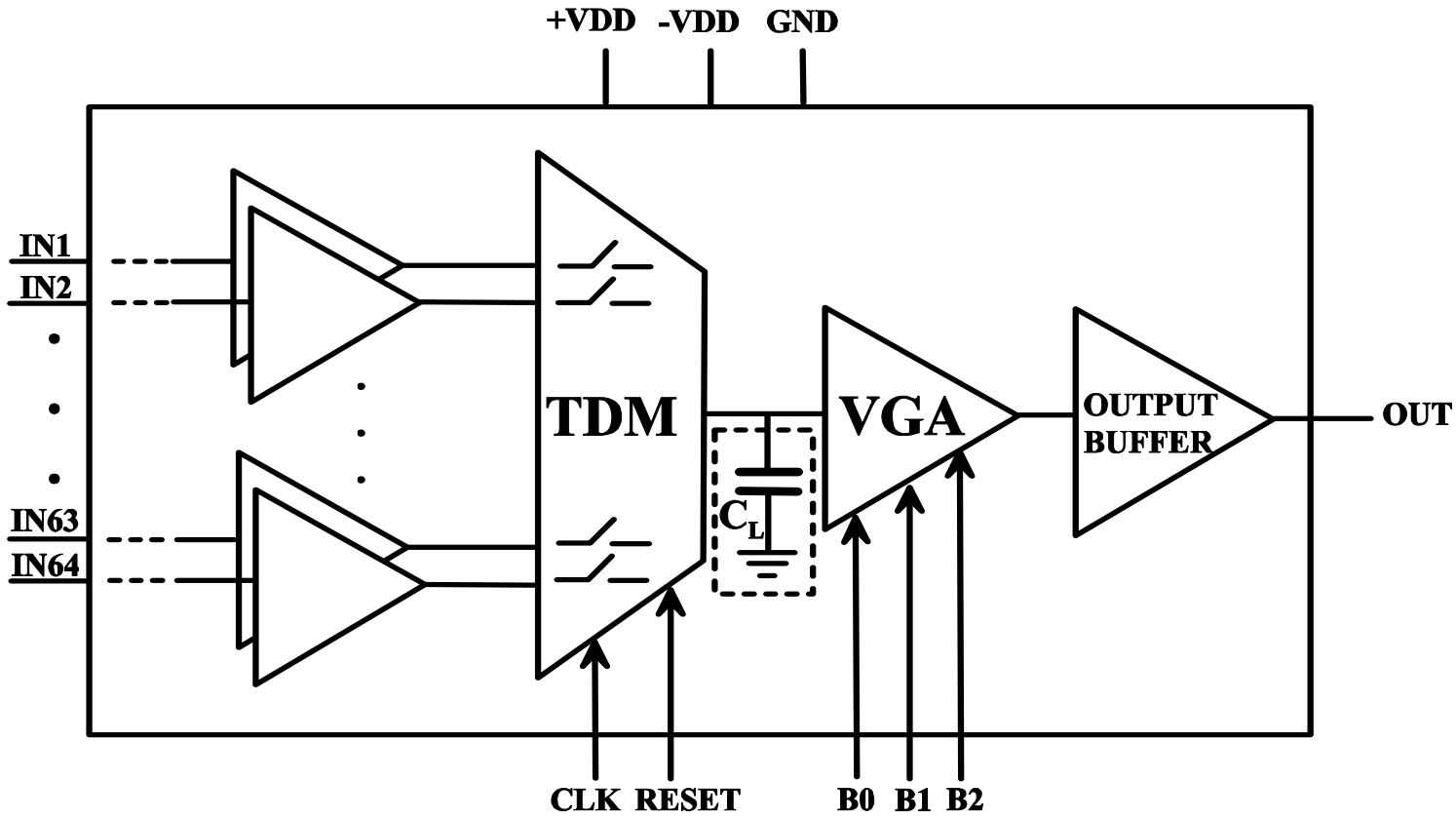
$C_2 = 200$ fF

Second stage



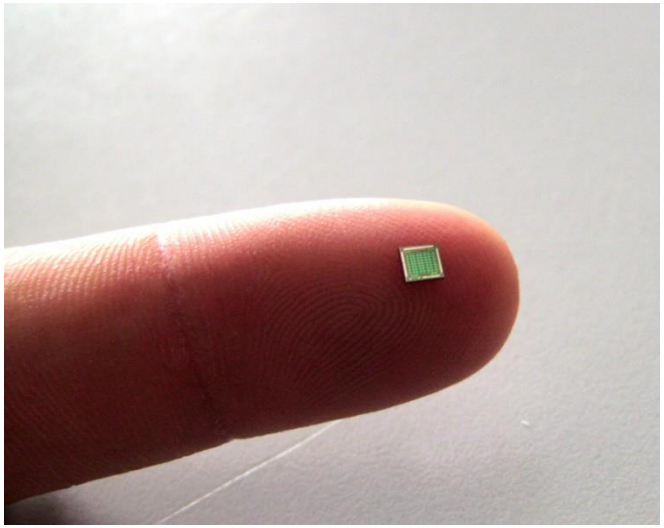
- DC offset removal
- Gain
- 2nd Order Pole Filtering

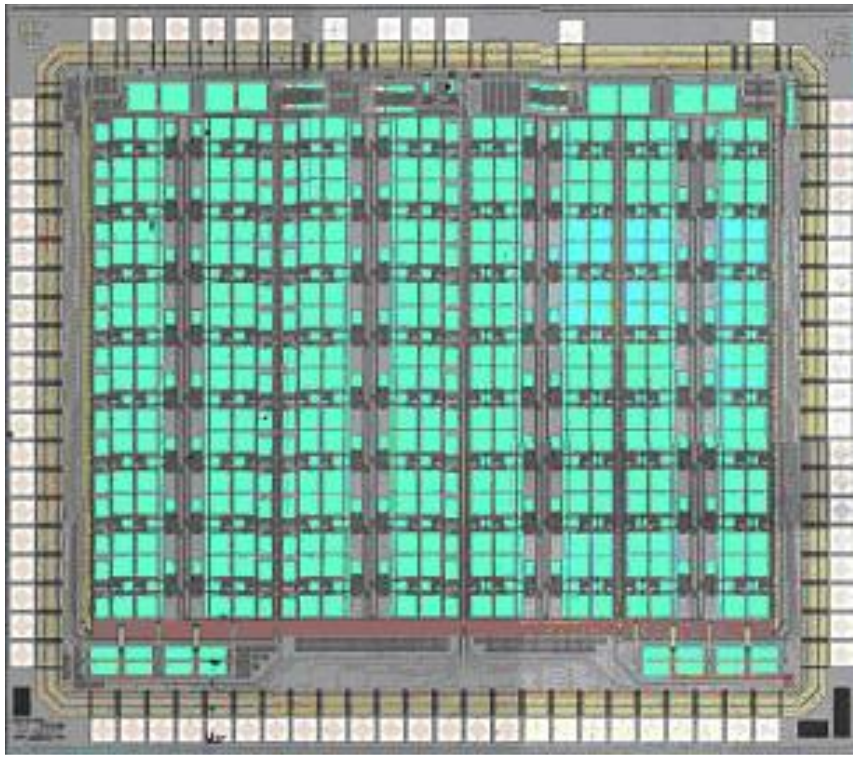
Array design



The chip

Fabricated in a 0.35-µm 2-poly, 4-metal commercial CMOS process through CMP





Dimensions: 2.6 mm x 3 mm

Characteristics

Technology	CMOS 0.35μm AMS
Chip Area	8.25 mm^2
Voltage Supply	± 1.5 V
Preamplifier midband gain	64 dB
Preamplifier bandwidth	2 Hz – 20 kHz
Preamplifier input noise (100 Hz – 10 kHz)	2.9 μV_{rms}
Buffer line settling time	100 nsec
Buffer output impedance	2 kΩ
VGA gain	0-27 dB
VGA + Output Buffer Bandwidth	> 10 MHz

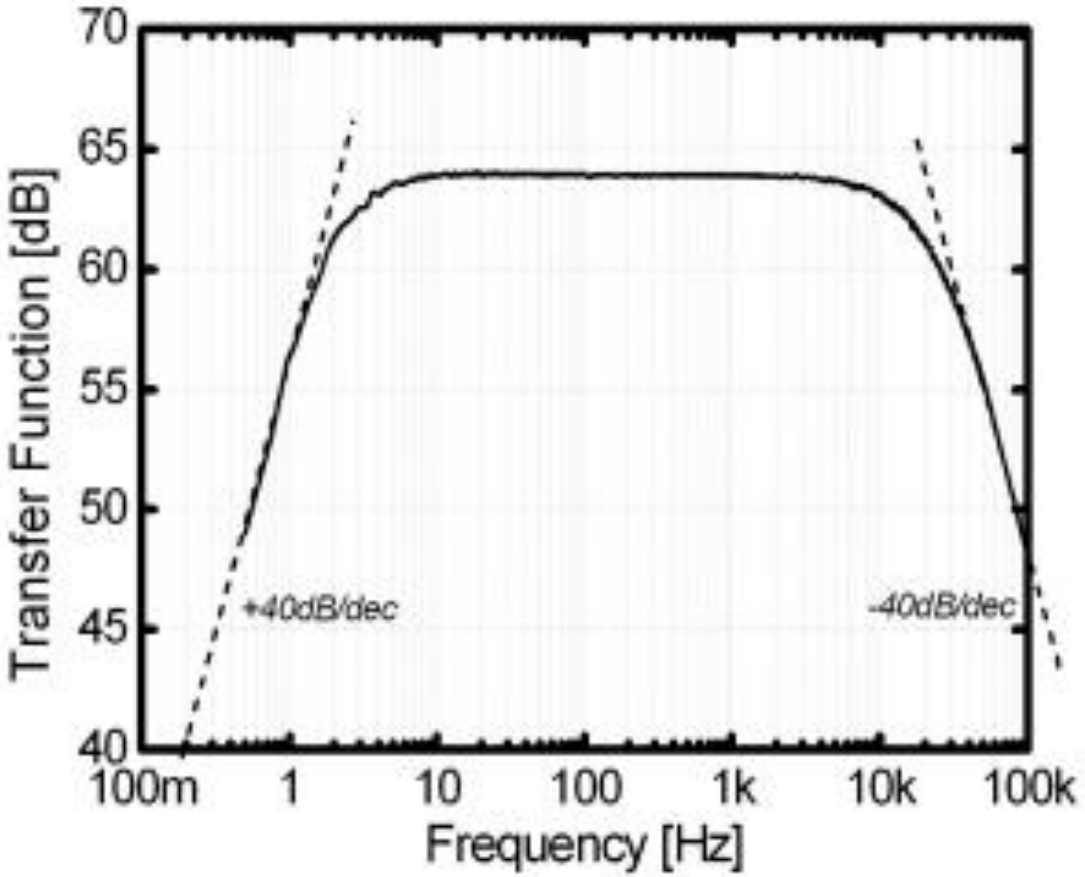
Power consumption (single channel)

Current consumption	
Preamplifer (each)	45 μA
Line Buffer (each)	45 μA
VGA Output	270 μA
Output Buffer	400 μA
Total	6 mA or 18 mW

More than 20 days of continuos recording with two AA battery

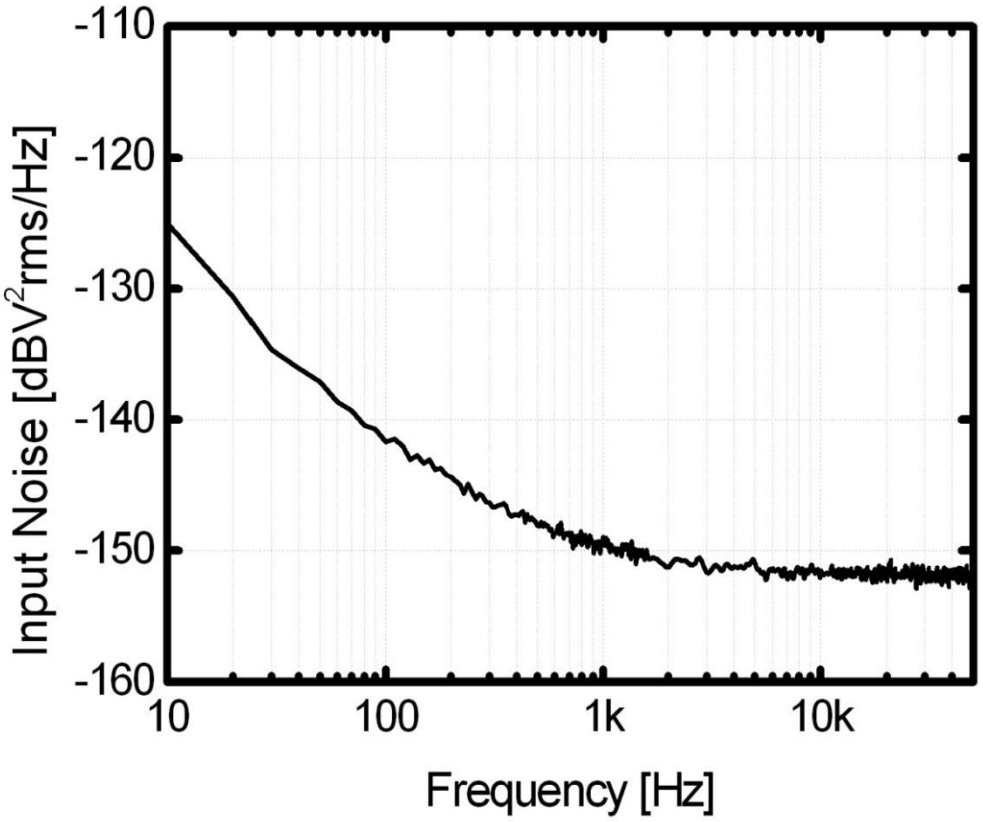
Experimental Results

Transfer function



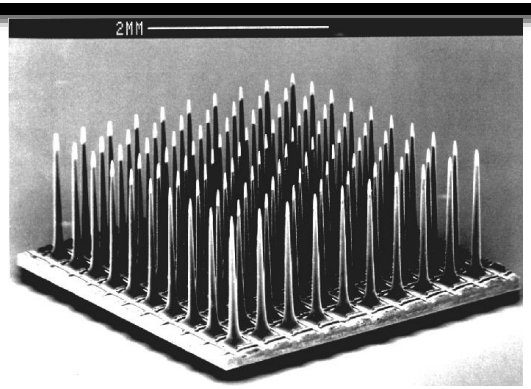
2nd order poles at 2 Hz and 20 kHz

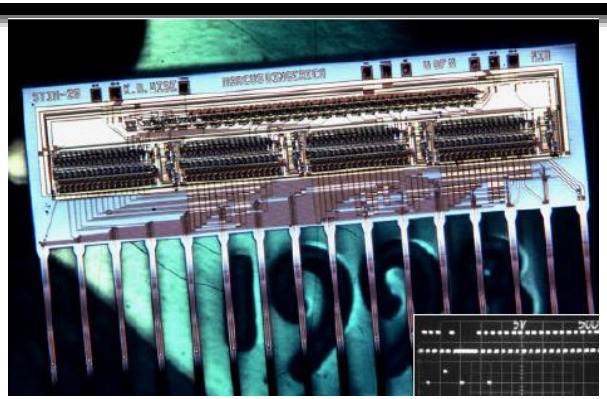
Noise performance

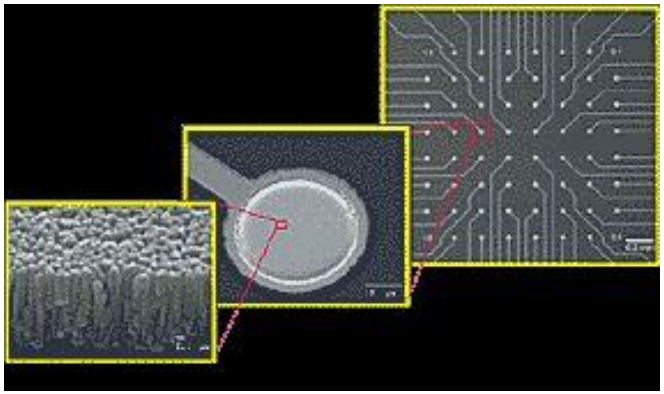


Input-referred rms noise of 2.9 µV (100 Hz – 10 kHz band) with 45 µA of current consumption

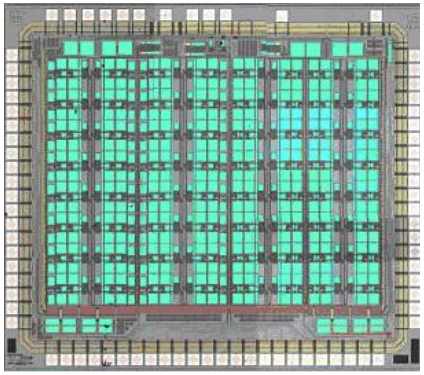
Commercial microelectrodes

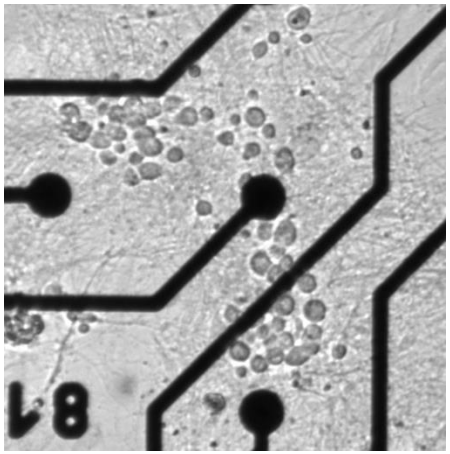


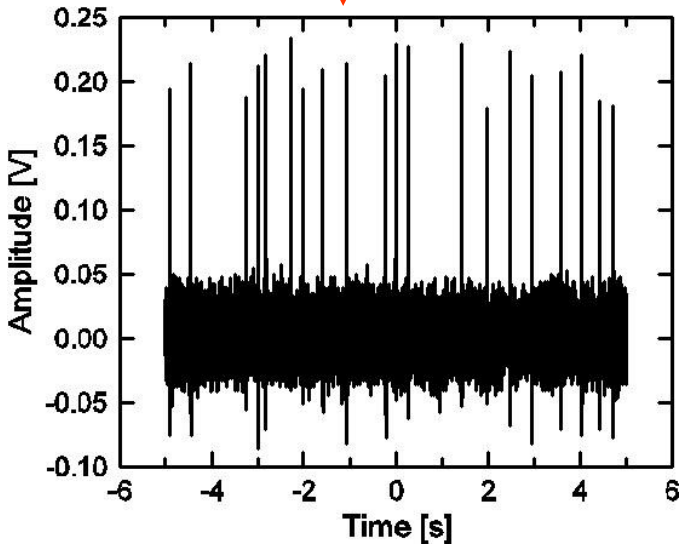




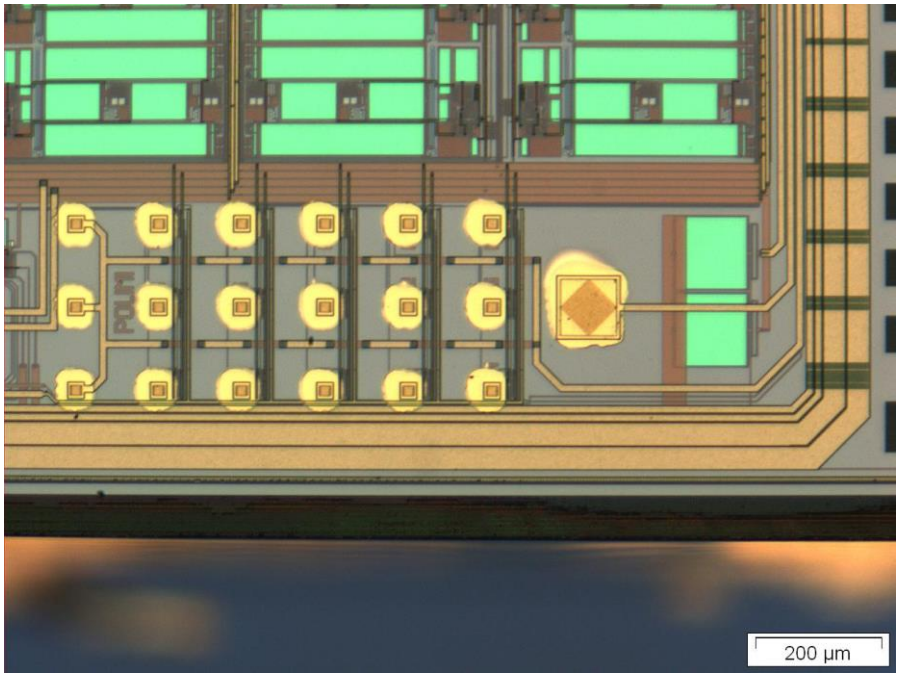
Preliminary recordings (*in vitro*)







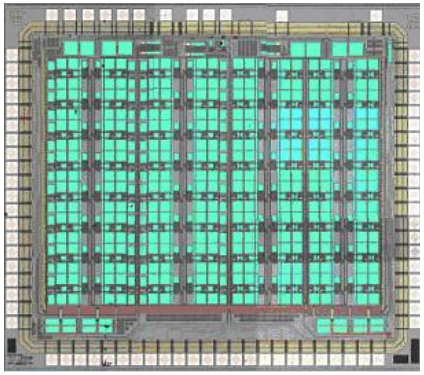
Electrode coating issue

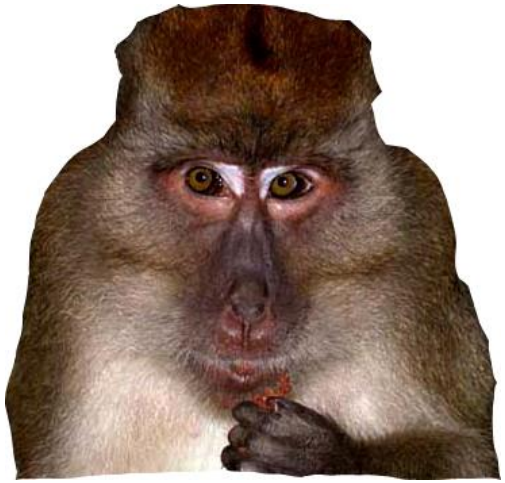


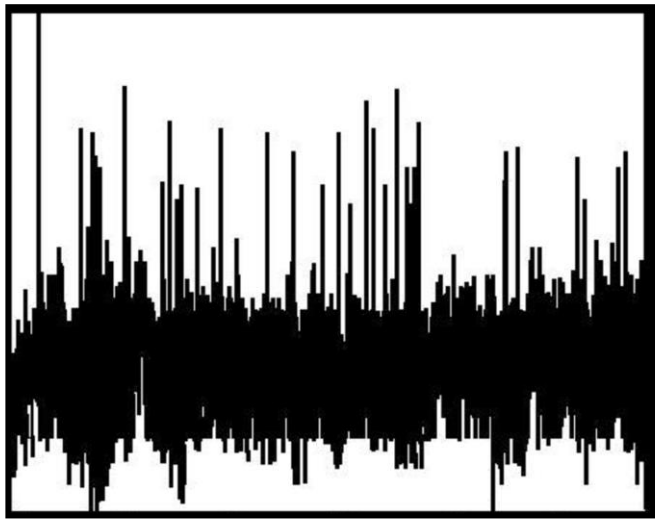
- 100 nm layer
- Mask resolution down to about 50 µm
- Lift-off technique with SU-8 masks

Electrode impedance endurance tests ongoing

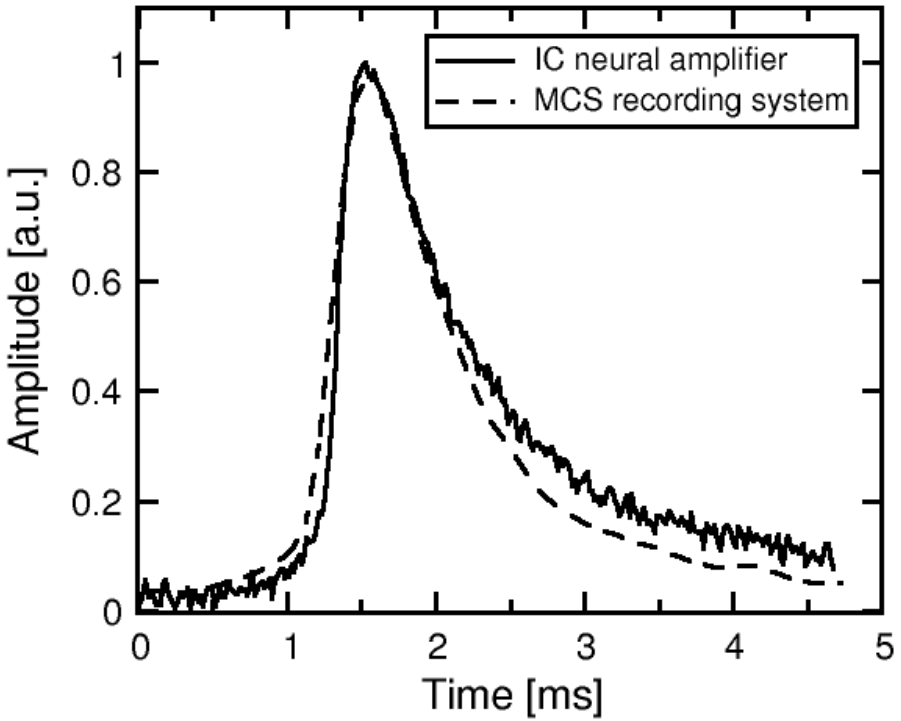
Preliminary recordings (*in vivo*)

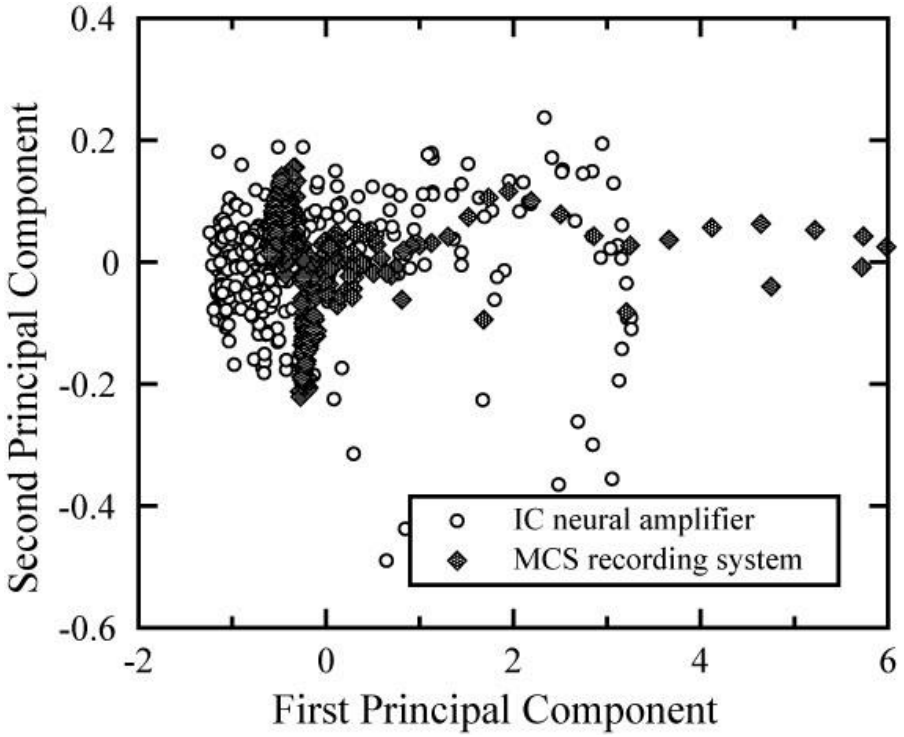






Quality of recorded data

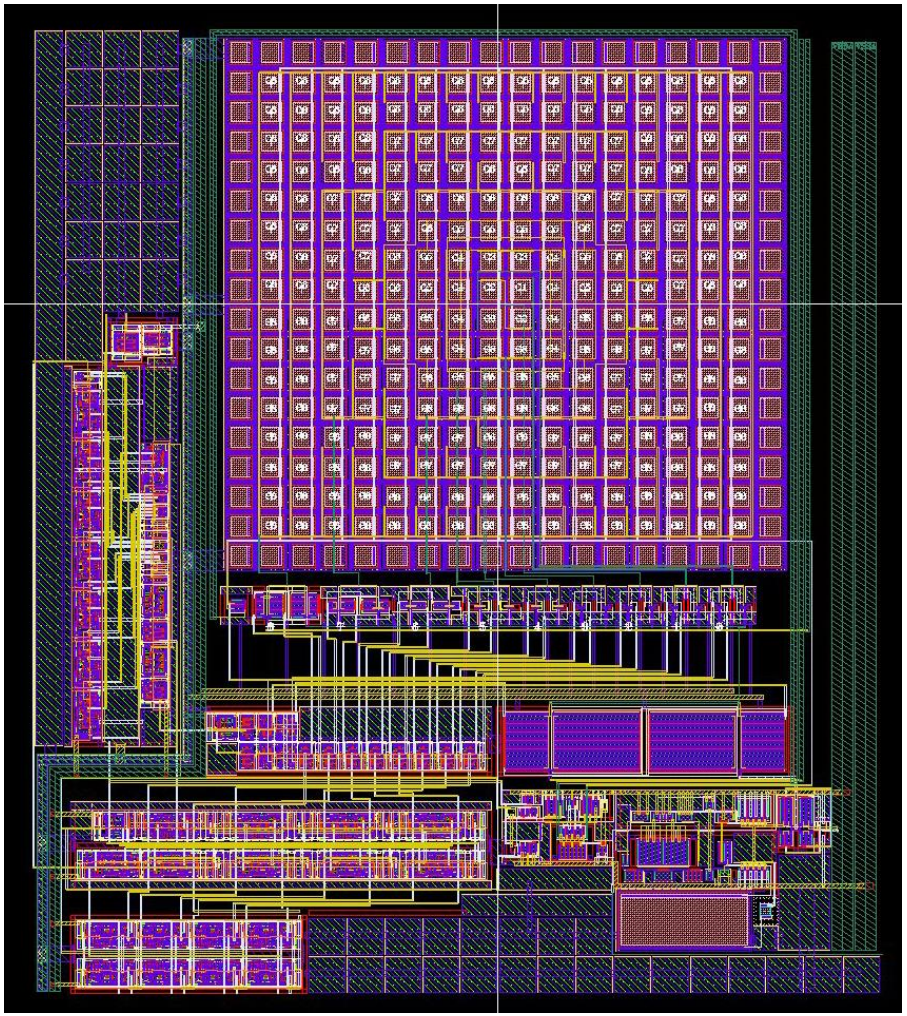




Achieved the same SNR and recording quality of bulky commercial systems (MCS)

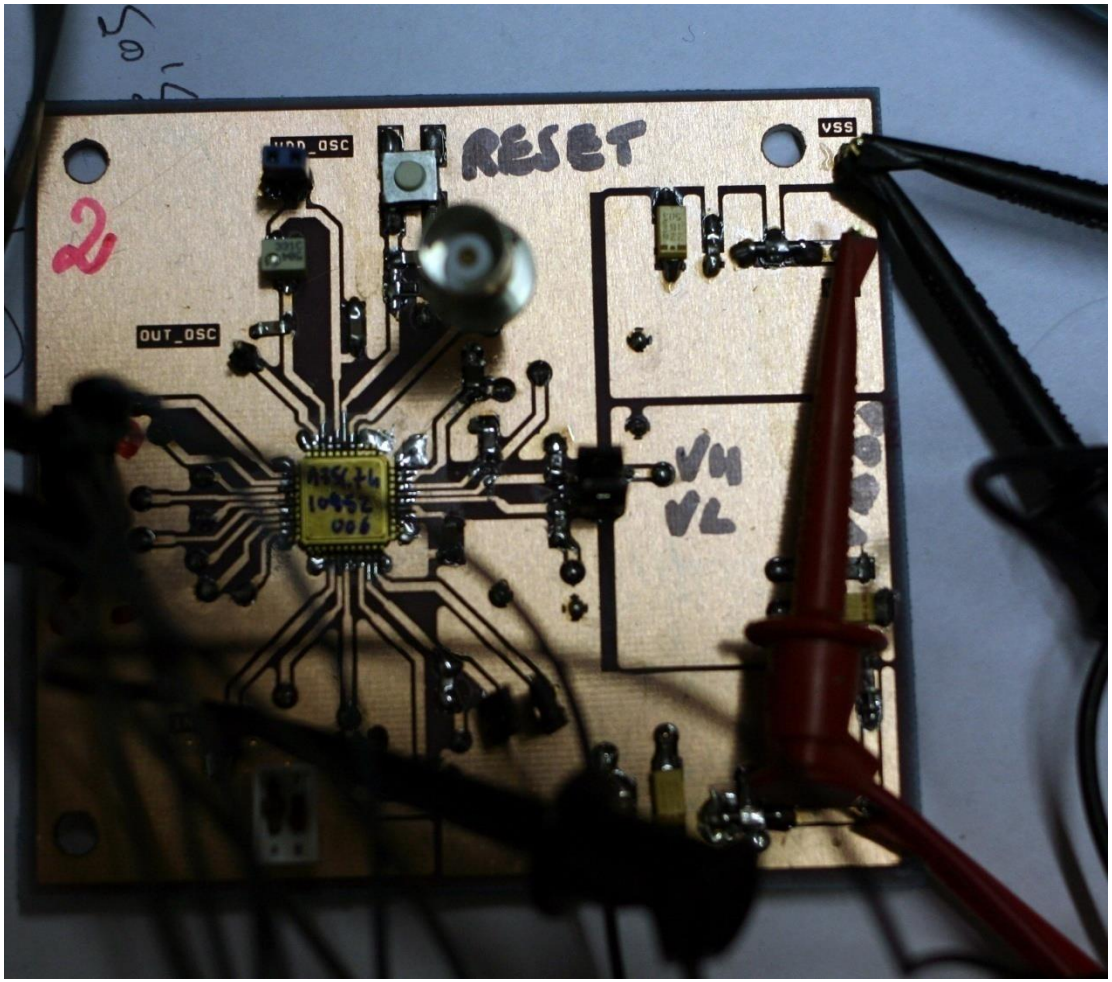
Ongoing Projects

8-bit SAR ADC

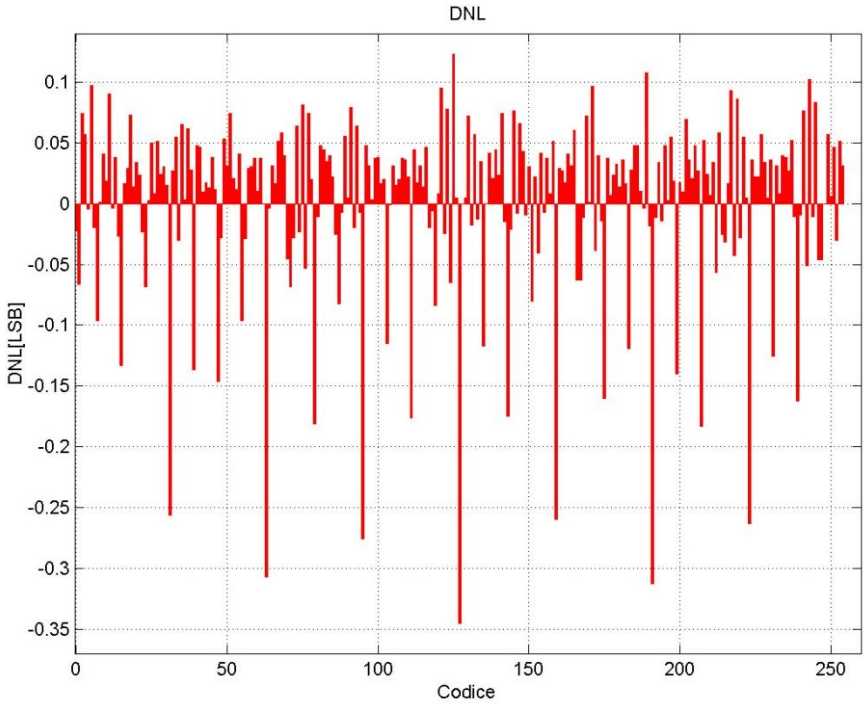


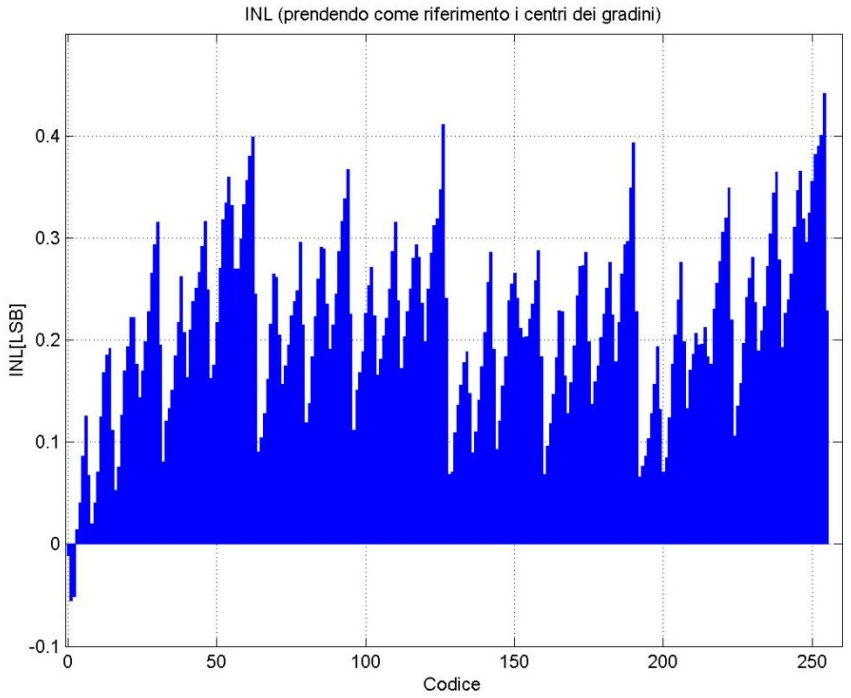
Parameter	Value
Supply voltage	3.3 V
Power	< 5 mW
Sampling Rate	1.28 MS/s (20 kS/s/Channel)
Clock Rate	20 MHz
Offset Error	< 1 LSB
V_{LSB} (electrode referred)	1 µV
Area in 0.35-µm Process	500 µm x 500 µm

ADC testing



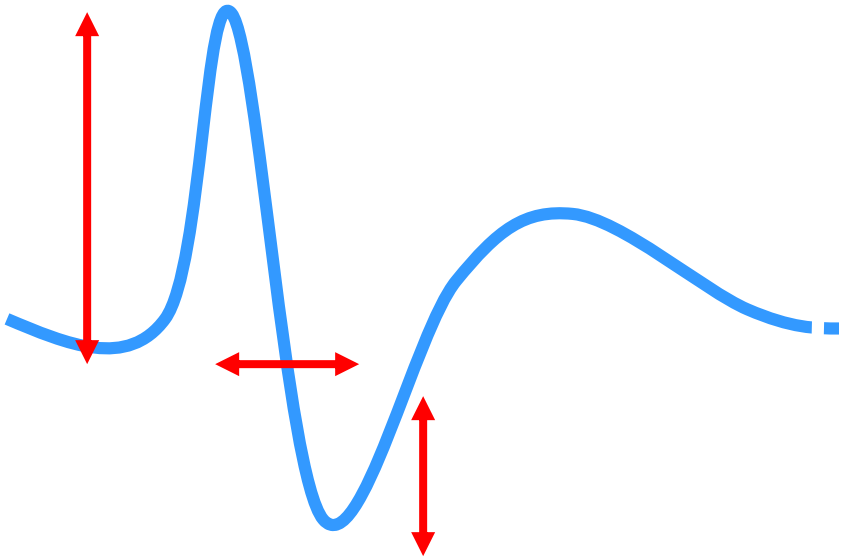
Preliminary results

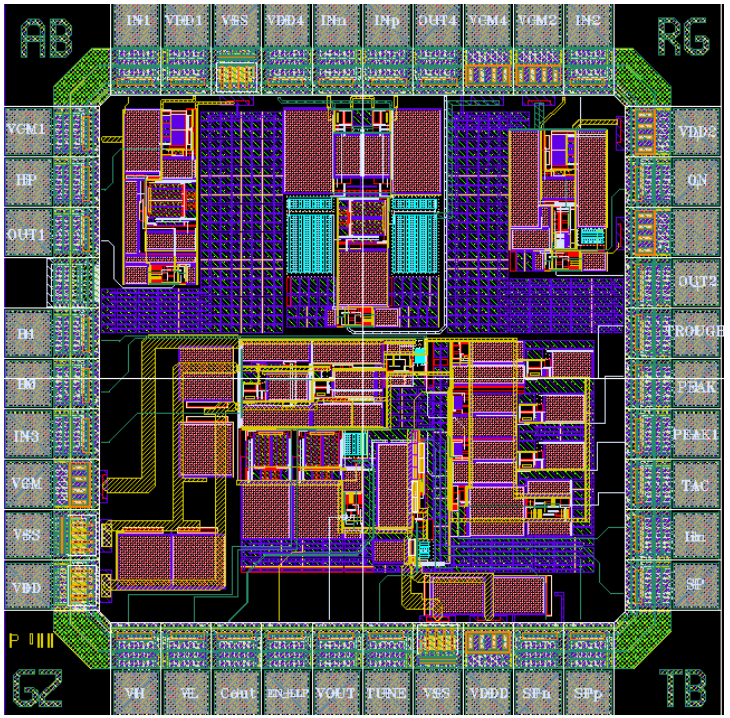




DNL < 0.4 and INL ≈ 0.4 LSB

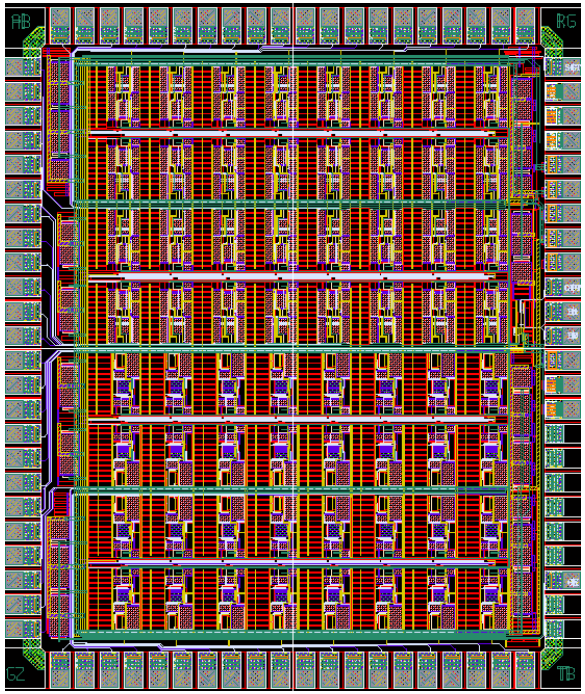
Analog sorting

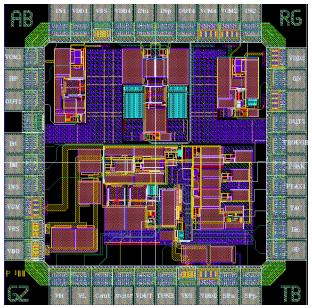


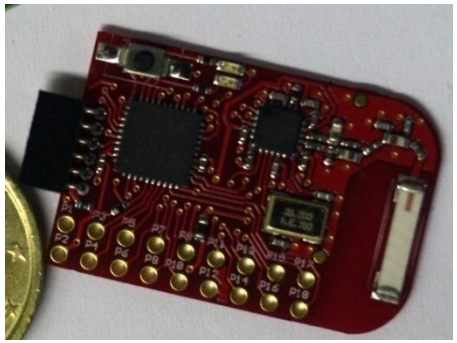


Low power consumption (300 µW)

Total power consumption







10 mW + 10 mW + 50 mW

Available power from inductive link ≈ 100 mW

Conclusions

- 64-channel array amplifier
  - Input referred noise of 2.9 V rms (lowest in literature)
  - Band-pass filtering from 2 Hz to 20 kHz
  - 60 db midband gain
- Good recording quality in field tests
- ADC under characterization
- Analog sorting designed (to be taped out)
- Digital processing, wireless transmission and power under study